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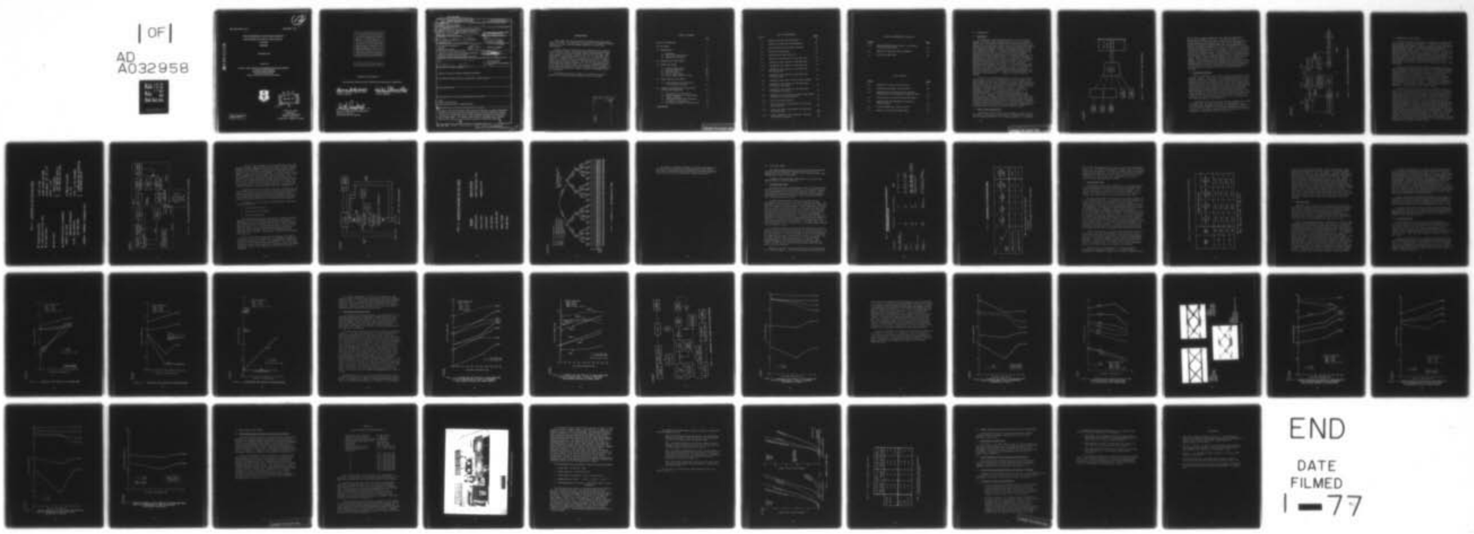

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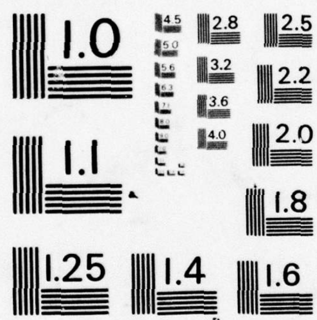

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CVSD PROCESSING OF QUASI-ANALOG SIGNALS IMPLICATIONS FOR TRI-TAC APPLICATIONS

VOLUME I

SUMMARY

OCTOBER 1976

Prepared for

DEPUTY FOR CONTROL AND COMMUNICATIONS SYSTEMS
ELECTRONIC SYSTEMS DIVISION
AIR FORCE SYSTEMS COMMAND
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In support of the USAF Program Office element of TRI-TAC, a series of laboratory and field environment tests were conducted by The MITRE Corporation to assess Continuously Variable Slope Delta (CVSD) modulation techniques for processing of quasi-analog signals. The results of these tests are presented in four volumes. This volume, Volume I, is an executive summary of all the test results.

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The test series documented here was sponsored by the USAF arm of the TRI-TAC Program: the Combat Theatre Communications Program Office, Electronic Systems Division, Hanscom Air Force Base. The encouragement and support provided by Lt. Col. H. Ellermets (DCJP) and Capt. T. Lindahl (DCJP) in the conduct of the tests and the timely test equipment and site arrangements made by Mr. W. Perling (DCJU) were particularly helpful. The authors also would like to acknowledge the support provided by Lt. Col. H. Ryan and his staff at the 102nd Air National Guard site at North Smithfield, Rhode Island where operational tests were performed; and the personnel at the Griffiss AFB DICEF where certain laboratory environment tests were conducted.

In addition we extend our thanks to the National Security Agency for providing the CVSD converters used in the tests.

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1.0 INTRODUCTION

1.1 Background

The development and phased-introduction of TRI-TAC digital systems into Combat Theater Communications involves an analog-to-digital (A-D) and digital-to-analog (D-A) conversion function for processing voice and quasi-analog signals for interface with digital switching and transmission systems. Continuously Variable Slope Delta Modulation (CVSD) is a currently favored algorithm for the voice conversion function. In TRI-TAC development programs, the CVSD algorithm has been selected for use in two new digital telephones; the Digital Non-secure Voice Telephone (DNVT), and the Digital Secure Voice Telephone (DSVT). An additional potential application for CVSD modulation is in the interfacing of inventory quasi-analog equipment with new digital systems. This interface function could be served by a family of TRI-TAC Universal Synchronous Multiplexers (USM) serving in a tactical channel bank configuration as suggested in Figure 1.1. The Air Force program office, in considering this interface function, did not have sufficient test data to determine the performance capabilities of CVSD in processing quasi-analog signals from various modems, voice encrypters and telephones f[illegible]terface with TRI-TAC digital systems.

In support of the USAF Program Office element of the TRI-TAC organization, a series of laboratory and field environment tests were conducted by The MITRE Corporation to assess CVSD processing of quasi-analog signals. The purpose of these tests was to assess the ability of delta modulator/demodulator devices to transmit various quasi-analog signals generated by existing U. S. Air Force equipment with sufficient fidelity to operate properly with interfacing systems. In cooperation with the USAF, a representative set of interfacing systems was identified and tested. The equipment included FSK and PSK modems, analog telephones and the Parkhill KY-65 voice encrypter. The test series was conducted over a 4-month period in FY'76 in several locations including a MITRE laboratory at Bedford, Massachusetts; the Combat Reporting Center (CRC) operated by the 102nd Air National Guard Unit at North Smithfield, Rhode Island; and the Digital Communications Experimental Facility (DICEF) at Griffiss AFB, New York.

1.2 CVSD - A Brief Explanation

The National Security Agency (NSA) provided the test item in the form of a full duplex unit which was configured with a current CVSD algorithm intended for voice signal application. In addition,

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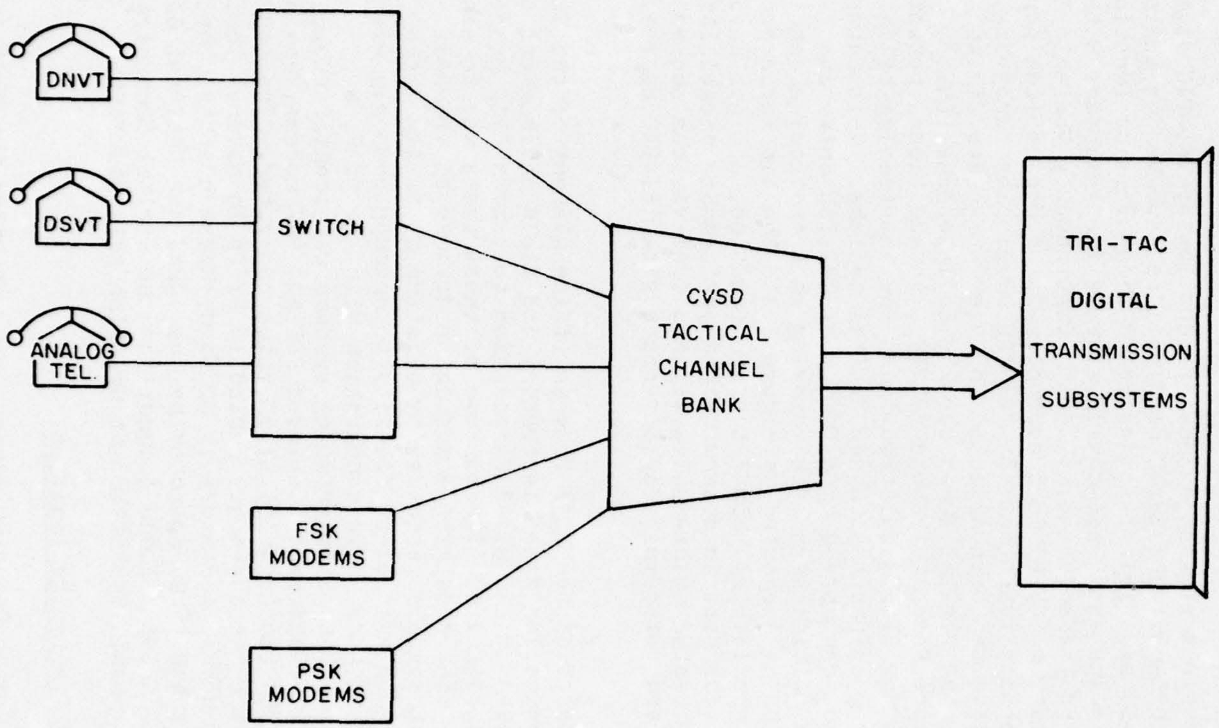

Figure 1.1 POTENTIAL TRI-TAC CVSD APPLICATION

an all digital commercial Adaptive Delta Modulator/Demodulator (ADM/D) was included in the tests. The ADM/D was built in accordance with current NSA specifications for the CVSD algorithm. In accordance with the NSA algorithm, the CVSD encoder shown in Figure 1.2 operates by comparing the input signal waveform at (A) with the feedback approximation (F) from the integrator. The output of the first register in the "run-of-three" counter is the digitized information transmitted at the clock (sample) rate and is a "one" if $A \geq F$ at the sampling instant. The amplitude of the feedback signal is derived by means of a three-bit shift register, logic sensing for slope overload, a pulse amplitude modulator and a syllabic low-pass filter. When a string of three consecutive "ones" or "zeros" appears at the output, a discrete voltage level is applied to the syllabic filter which changes the feedback pulse amplitude until the overload string is broken. Amplitude change polarity is controlled by the output of the first bit register. The decoding process at the receive end is essentially the reverse of the foregoing encoding.

1.3 Information Presented

The data collected in this series of tests is presented in four volumes. Volume I, this volume, is a condensed version of the more detailed information contained in the other volumes, and as such it constitutes an executive summary of the results of this test series. Volume II presents the detailed results of the tests conducted with the NSA CVSD units, and Volume III contains all of the data gathered in a similar set of tests performed on a commercially developed adaptive delta modulator/demodulator (ADM/D) unit designed to the same algorithm as the NSA CVSD. Volume IV describes the tests run on the Parkhill KY-65 voice encrypter with both the NSA CVSD and the commercial ADM/D. Also included in Volume IV are the results of tests run on a hybrid setup using the NSA CVSD as a modulator and the commercial ADM/D as the demodulator.

A description of the test series and test equipment is provided in Section 2.0. The modem test series and some special tests involving tandem multiple conversions are documented in Section 3.0 and the results of DTMF tests with analog telephones are given in Section 4.0. The overall conclusions and implications for TRI-TAC application of CVSD are provided in Section 5.0.

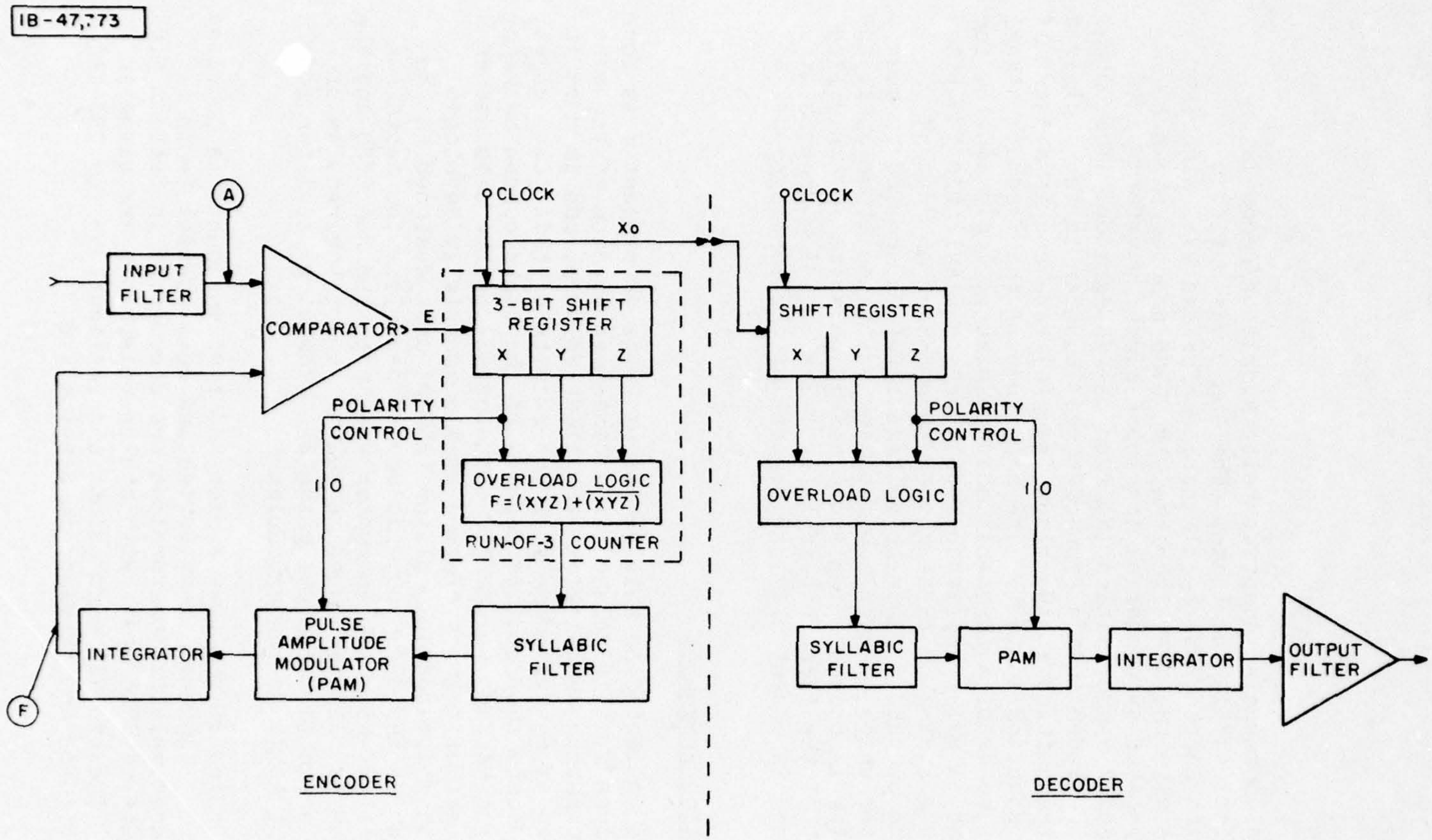

Figure 1.2 TYPICAL CVSD MODULATOR AND DEMODULATOR

2.0 DESCRIPTION OF TEST SERIES

The CVSD test series was conducted to provide a sufficient data base to allow a technical evaluation to be made of the ability of delta modulator/demodulator devices to transmit various quasi-analog signals generated by inventory equipment which may interface with TRI-TAC digital systems. The tests conducted by MITRE can be categorized into three subsets: 1) Modem interfaces, 2) Dual Tone Multiple Frequency Signalling and Supervision, and 3) Parkhill (KY-65) Voice Encrypter. Due to the sensitivity of information on Parkhill performance, test results on that particular CVSD interface are presented in a separate volume, Volume IV, of this report. The test objectives for each of the subsets are set forth at the beginning of each section dealing with the particular tests to which they apply.

After the objectives had been stated, the parameters of test were established. These parameters and the nominal variation ranges (where applicable) are provided in Table 2.1. The manner in which the parameters were controlled and the specific interfacing device parameter values were influenced by anticipated operational requirements and the characteristics of the particular inventory item for the CVSD interface. Detailed descriptions of the test configurations and inventory item characteristics are provided in other sections of the paper; however, representative configurations for each of the test subsets cited above are presented here for purposes of illustrating the general test setup.

In general, the modem test subset was configured as shown in Figure 2.1. A random bit generator was used to form the information data stream which constitutes the input to the modem's transmitter. A pad at the transmitter output provided a means of modifying the input signal level of the CVSD encoder. The sample rate for the conversion process was controlled by the clock. The rates used in each test were 32 and 16 kb/s. A bit error generator provided levels of background and burst errors which were injected into the independent channel. The error rates which were utilized generally bound tropospheric models which are gaining TRI-TAC acceptance. A unit amplifier at the reconverted audio output of the CVSD decoder provided line level compensation for the modem receiver. The output of the modem receiver was compared with the information bit stream transmitted, and errors were indicated on a counter or hard copy printer. Thus, this configuration provided a direct method of deriving bit error rates from the CVSD process under known noise and signal level conditions. Loop variations, if utilized, were applied downstream of the CVSD conversion process.

TABLE 2.1 PARAMETERS OF TEST FOR FIELD SERIES

● SAMPLE (CLOCK) RATE	16 KBS, 32 KBS
● SIGNAL LEVEL AT CVSD INPUT	0 DBM -30 DBM (DISCRETE)
● BIT ERROR RATES	BACKGROUND: 10^{-4}, 10^{-3}, 10^{-2}
	BURST: 2×10^{-2}
● LOOP PATHS	A. BACK TO BACK B. LOOP THROUGH TROPO IF C. LOOP THROUGH GCC-6 MUX
● INTERFACING DEVICE PARAMETERS	
MODEM: BAUD RATE	75-2400 BPS (DISCRETE)
MODULATION TECHNIQUES	FSK, PSK
TA-341: TONE DURATION	50 MS - 1.4 SEC (DISCRETE)
DUAL TONE RANGE	A. SIGNALLING AND SUPERVISION B. TONE PAIRS FOR 0-9
PARKHILL: PREAMBLE, SCRAMBLED VOICE	

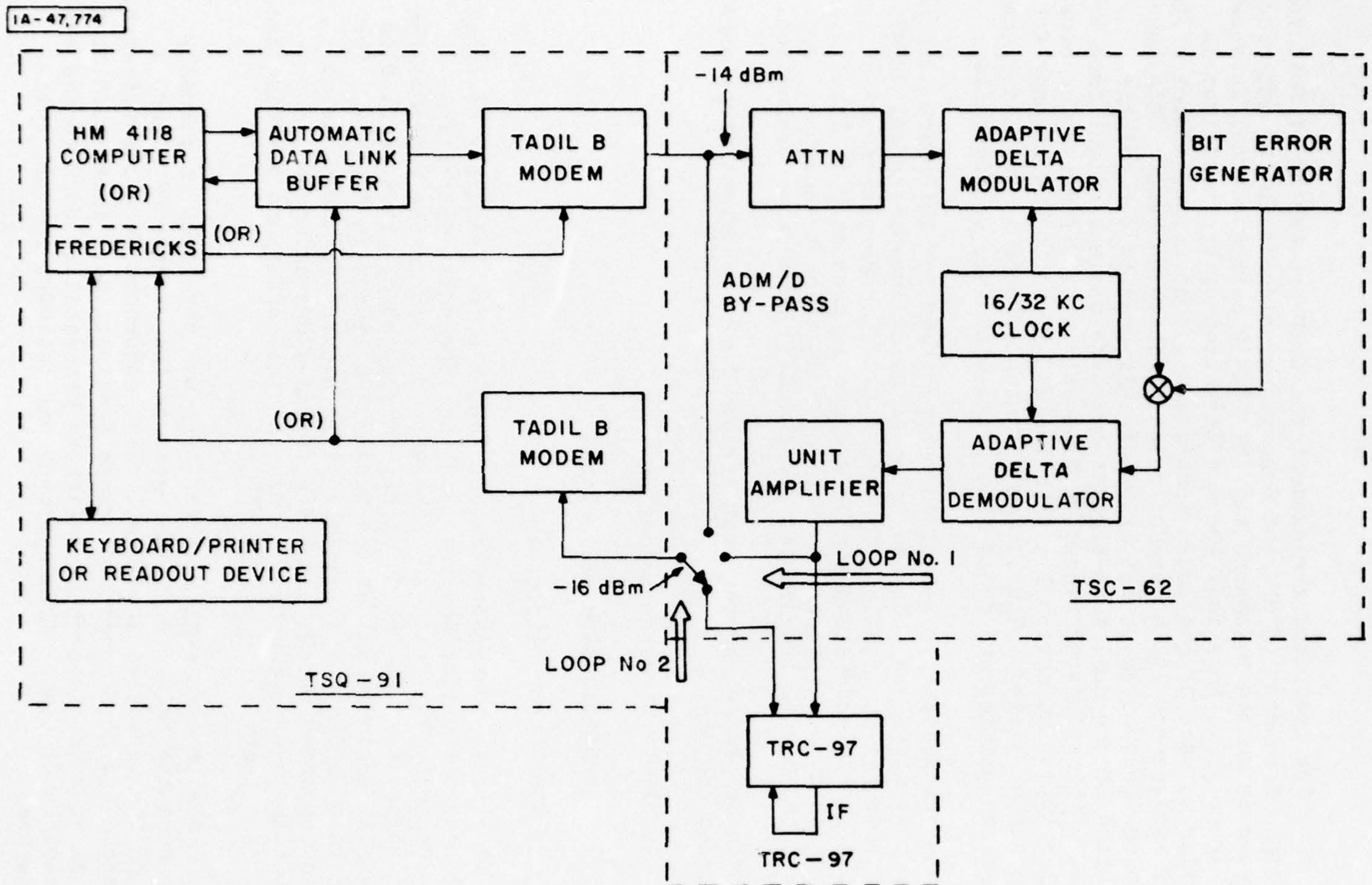

Figure 2.1 TEST CONFIGURATION FOR TADIL-B TESTING

The test item arrangement for CVSD processing of Dual Tone Multiple Frequency (DTMF) and Supervisory signals in the interface between an analog telephone and the TTC-30 switch central is shown in Figure 2.2. Note that the configuration of the test item is similar to that of the modem arrangement. One unique aspect of the DTMF arrangement is the use of pulse duration control. This special test equipment item, built by MITRE, was used to control the duration of the dual tone signals (numbers dialed) output from the phone. Pulse lengths ranged in discrete levels from a value close to the 40 ms detection limit of the TTC-30 up to 1.4 seconds for each number dialed. Thus, tone duration effects as well as signal level and sample rate could be studied with this configuration.

A representative set of inventory items for interface with the CVSD converters was selected using as guidelines potential TRI-TAC architectural applications for the A-D/D-A conversion function. A list of these modems and analog devices is presented in Table 2.2. The selected devices offered various modulation techniques, baud rates, and signal frequencies for the CVSD processing evaluation.

In preparing for the test series, three important steps were followed comprising:

1. Pretest characterization

2. Identification of variables

3. Test tree development

The pretest characterization consisted of frequency response, amplitude distortion analysis and envelope delay distortion measurements. The test variables were derived on the basis of the test objectives and the inventory devices used. These variables generally included all of the parameters listed in Table 2.1 for each test series. Some variations in parameter values shown, including added parameters, were utilized depending on the particular test conducted. These special conditions are discussed with each test.

Prior to each series a test tree was developed to formally structure the test. As illustrated in the example of Figure 2.3, all of the variables are shown. Test sequences were identified by reference to tree nodes and branch terminations. Thus, each test was given a unique number permitting traceability back to the exact parameters of test. This approach was followed for all tests conducted.

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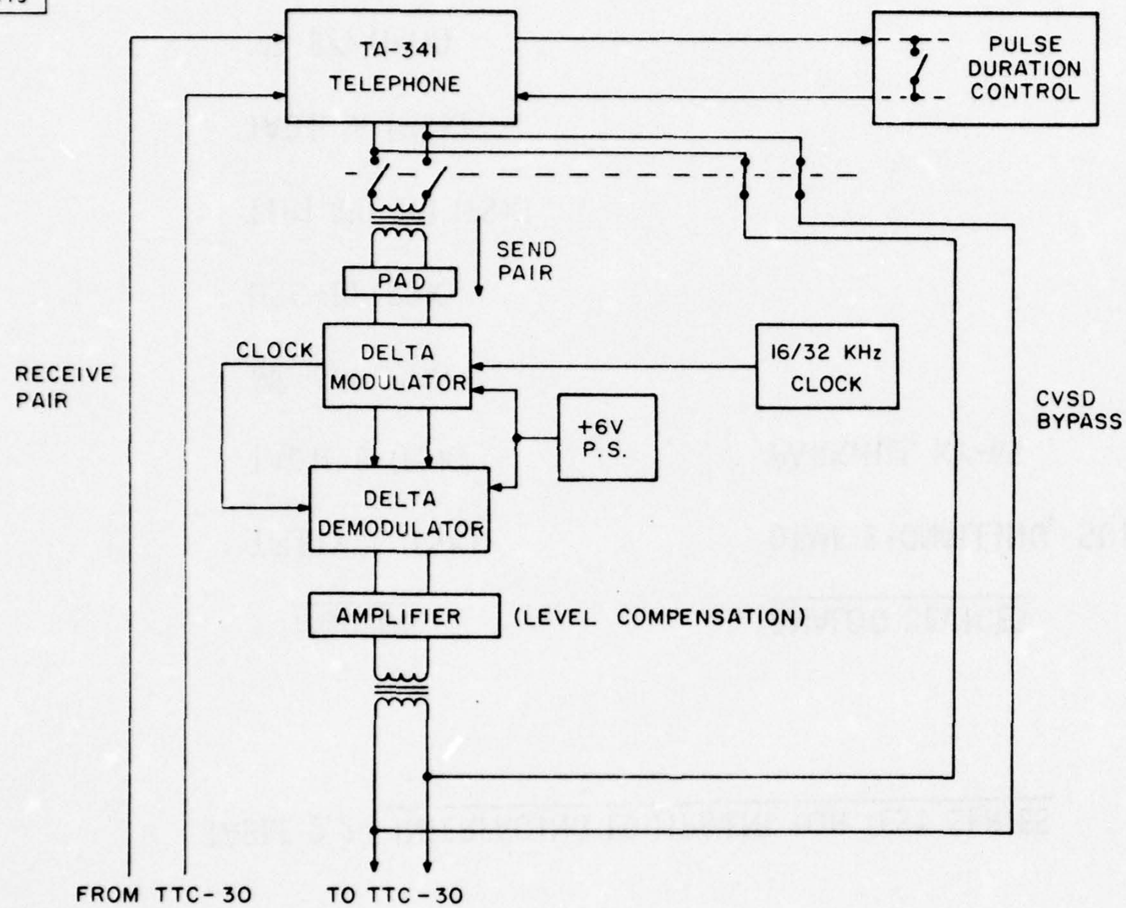

Figure 2.2 DTMF TEST CONFIGURATION

TABLE 2.2 INTERFACING EQUIPMENT FOR TEST SERIES

MODEMS	ANALOG DEVICES
TELETYPE (FSK)	DTMF SIGNALLING, SUPV.
TADIL B (FSK)	PARKHILL KY-65
MD-674 (FSK)	
USC-10 (PSK)	
TIPI MD-701 (FSK)	
TADIL A (PSK)	
MD-823 (PSK)	

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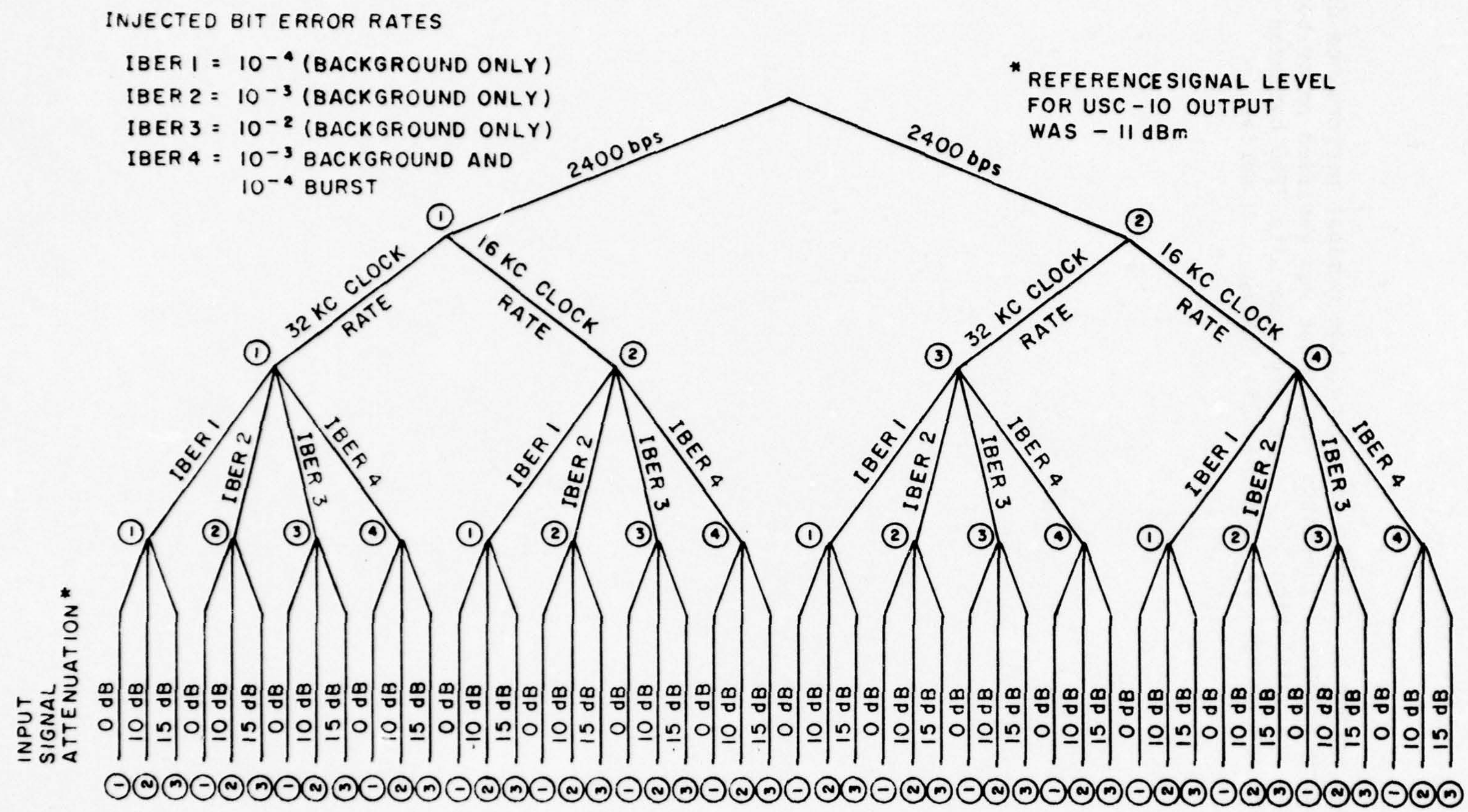


Figure 2.3 **AN/USC-10 — PSK MODEM TEST TREE**

As a matter of general procedure, the nominal performance of interfacing field and laboratory equipment was verified prior to each test and validation test runs were made with CVSD bypassed at the start of the test and periodically during each series.

3.0 MODEM TEST SERIES

The signal sources chosen for the modem test series represent both FSK and PSK modulation techniques and provide for the examination of the conversion process over a variety of data rates ranging from 75 baud to 2400 baud.

A summary of the principal characteristics of each of the modems tested is listed in Table 3.1.

3.1 Teletype Modem Tests

The objective of the Teletype Modem Tests was to establish how successfully low baud rate FSK modulated, voice frequency signals could be processed by the CVSD A/D/A conversion process. The TTY test series was conducted at the 102nd Tactical Control Squadron, Air National Guard, North Smithfield, Rhode Island, on November 18th, 1975 and January 6th, 1976.

The data stream source for testing the effects of CVSD processing on TTY signals was a DAC-8 TTY Character Generator. The mark/space currents produced by the DAC-8 were used by a KY-664 Tone Keyer to produce 75 baud FSK signals. These signals were processed by the CVSD encoder and decoder and the resulting FSK signals were converted back to mark/space format by the CV-2543 Tone Converter. The output of the CV-2543 unit was used to drive a teletype page printer and TTY distortion analyzer. The distortion analyzer indicated the sense and magnitude of switching and mark/space bias distortion. The output of the teletype page printer was examined to establish if erroneous characters had been developed due to data errors resulting from the A/D/A process. The output signal level of the Tone Keyer was set at -12 dBm which is a nominal operating value used in the 407-L system.

In this test series two data paths were tested; one from the output of the A/D/A process directly back to the Tone Converter, and one path from the A/D/A process through the TRC-97 Radio Set back to the Tone Converter. In the loop through the TRC-97, the processed FSK signal was stacked in frequency with 15 other TTY circuits into one voice channel. That voice channel in turn was frequency multiplexed with 23 other channels onto an IF carrier. The transmitter signal at IF was then patched into the appropriate receiver channel and the resulting demultiplexed signal was sent back to the tone converter.

Table 3.2 shows the results obtained from the CVSD processing of the Teletype Signals. No errors were observed at either the 16

Table 3.1 CHARACTERISTICS OF MODEMS USED IN TESTING TRANSMISSION OF DATA SIGNALS PROCESSED BY CVSD

NOMENCLATURE	BIT RATE (B/S)	MODULATION TECHNIQUE	NOTES
KY-664 (TONE KEYER) CV-2543 (TONE CONVERTER)	75	FSK	FM = 1225 HZ, FS = 1325 HZ
TADIL-B (MD 807)	600	FSK	FM = 1300 HZ, FS = 1700 HZ
	1200	FSK	FM = 1300 HZ, FS = 2100 HZ
AN/USC-10	1200	PSK	UPPER, LOWER TONE LIMITS: 715-1485 HZ
	2400	PSK	UPPER, LOWER TONE LIMITS: 715-2475 HZ
MD-823 (IC CORP., BELL 201)	2400	4ϕ PSK	BANDWIDTH 1200-2400 HZ
MD-701 (LENKURT 26C)	1200	FSK	FM = 1200 HZ, FS = 2400 HZ
	2400	DUOBINARY FSK	FM = 1200/2400 HZ, FS = 1800 HZ

Table 3.2 **PERCENT ERRORS IN CVSD PROCESSED TTY SIGNALS**

BER / SAMPLE RATE	10^{-4} background only	10^{-3} background only	10^{-2} background only	10^{-3} background & $2x10^{-2}$ burst	10^{-3} background & $2x10^{-1}$ burst
Message Errors at 16 kb/s	0 %	0 %	0 %	0 %	100 %
Message Errors at 32 kb/s	0 %	0 %	0 %	0 %	100 %

Note: Conclusions apply to both loops tested

1) Back-Back

2) Loop-up through GCC-6, & TRC-97 to if and return

kb/s or 32 kb/s sampling rate for either loop for most background error rates. The effects of reducing the signal level into the CVSD encoder over the range from -12 dBm to -30 dBm produced no recorded errors in the output text. The only errors observed occurred for a background error rate of 10^{-3} and a burst error rate of 2×10^{-1}. At this rate, a very extreme error environment, the teletype printer's output was completely incorrect.

3.2 TADIL-B Modem Tests

The objective of the TADIL-B modem tests was to establish how accurately medium baud rate FSK modulated voice frequency signals could be processed by the CVSD A/D/A conversion technique. The TADIL-B modem tests were conducted at the 102nd Tactical Control Squadron, Air National Guard, North Smithfield, Rhode Island, on November 25th, and December 4th, 1975 and January 7th, 1976.

The data stream source for testing with the TADIL-B modems was an HM-4118 computer system. The computer output was coupled to the TADIL-B modem by means of an automatic data link buffer. The purpose of the buffer was to access the computer's memory at a data rate dictated by the modem, and to perform the parallel to serial data conversion. The output of the TADIL-B modem was an FSK signal at 600/1200 BPS into a 600Ω load. After A/D/A processing by the CVSD system, the processed FSK signal was converted back to a serial data stream by the TADIL-B receiver. The serial data stream was converted to parallel format and stored in the HM-4118's memory. The processed results were compared with the transmitted message, and the the computer maintained a running account of the number of valid messages received and the number of received messages in which the data was in error. In the 72-bit transmitted message 24 bits represented prelude and framing. If these bits were correct, the message was declared valid; if the remaining 48 data bits matched the transmitted data word, the message was considered error free.

In this test series, as in the TTY test series, two data paths were tested. The first path returned the data directly to the TADIL-B receiver after CVSD processing. The second path returned the data to the TADIL-B receiver by way of the TRC-97 Tropospheric Radio Set. In the loop through the radio system the same path as described in the TTY test was followed with the exception of the first 16:1 multiplex step. The output of the TADIL-B transmitter was set at -14 dBm to conform to standard site practice.

The results of CVSD processing on the TADIL-B modem's performance is summarized in Table 3.3. This performance is described for a series of inserted digital errors, at both 16 and 32

Table 3.3 Percent Error Free Messages in Processed TADIL-B Signals

SAMPLE RATE	BAUD RATE	INJECTED BIT ERROR RATE			
		10^{-4} (background only)	10^{-3} (background only)	10^{-3} background & $2x10^{-2}$ burst	10^{-2} (background only)
16 kb/s	600	99.95*	98.10	97.40	97.70
	1200	99.80	98.80	97.00	87.60
32 kb/s	600	100.00	100.00	99.94	100.00
	1200	100.00	100.00	99.94	99.93

*Values are for % Error Free Messages Received

NOTE: Input Level to CVSD: -14 dBm, 600 Ω

kb/s for the two baud rates tested. This table provides a loop quality indication based on the percentage of error free messages received as a function of the total number of messages received. It should be noted that this table describes a summary of the modem's performance at the nominal operating level of -14 dBm. Because of the sensitivity of the CVSD conversion process to input signal level, the modem's performance was degraded in all instances as the input signal level to the CVSD encoder was decreased from this nominal input level. At the 32 kb/s sample rate the deterioration in performance was most dramatic from -24 dBm to -32 dBm with little change in recorded error rates occurring from the -14 dBm to -24 dBm signal levels. The observed data error rates at the 16 kb/s sampling rate were higher at all signal levels than those observed at 32 kb/s. When the TRC-97 Radio System was inserted into the loop between the CVSD process and the TADIL-B receiver, results almost identical to those shown in Table 3.3 for the direct path were obtained.

3.3 PSK Modem Tests

The objective of this series of tests was to establish with what degree of success high baud rate PSK modulated voice frequency signals could be processed by the CVSD A/D/A conversion technique. In this test series two PSK type modems were investigated: the AN/USC-10 and the MD 823. The two modems were tested in a laboratory environment at the Digital Communications Experimental Facility (DICEF), Rome Air Development Center (RADC), Griffiss Air Force Base, New York, on December 9th, 10th and 11th, 1975.

In the test configuration used to establish the effect of CVSD processing on modem performance with these units, an ICC Model 110B Transmission Set was used as the data test generator and receiver. A pseudo-random digital bit stream generated by the transmission set was converted to PSK format by the modem under test. The AN/USC-10 modem was adjusted for -11 dBm output while the MD-823 was operated at the 0 dBm point. After passing through the CVSD units, the PSK signal was then processed by the receiving modem to produce a digital bit stream that corresponded with the original output of the transmission set. A pattern synchronizer was used to compare a delayed version of the transmitted data bit stream to the received data bit stream. Errors resulting from differences between the two processes were recorded on a VALVO Error Counter. This counter maintained a record of the number of message blocks sent, the number of bad message blocks received and the number of individual errors detected. A message block in this context is 2047 bits in length, and a bad message block is defined as having at least one error.

A graphical presentation of the range of performance obtained for the AN/USC-10 modem employing a CVSD modulator as the A/D/A conversion process is provided in Figures 3.1 and 3.2. These curves show the effects of bit error rates (BER) in the independent channel on the CVSD output bit error rate as a function of attenuation of the CVSD input. Injected bit error rate conditions, labeled IBER 1 through IBER 4, refer to the levels of background (bg) and burst (bst) errors introduced into the independent channel in the transmission process. Performance data is shown for both 16 and 32 kb/s clock rates. The former figure describes the data at a 1200 baud data rate while the latter shows the same data at the 2400 baud rate. It should be noted that synchronization could not be obtained between the transmitting and receiving modems at the 16 kb/s clock rate for data transfers at the 2400 baud rate.

Figure 3.3 provides a graphical presentation of the range of performance obtained for the MD-823 modem when the CVSD process was employed as the A/D/A conversion technique. The MD-823 modem was tested only at a 2400 baud rate, and measurements at the 16 kb/s sample rate were made only for the operating signal level of 0 dBm.

It should be pointed out before leaving this test series that the results of using CVSD as a conversion process with PSK modems is highly dependent not only on the sensitivity on input amplitude as demonstrated for FSK modems but also on the phase linearity of the elements of the conversion process.

3.4 MD-701 Modem Tests

The objective of this test series was to establish how successfully high baud rate FSK modulated voice frequency signals could be processed by the CVSD A/D/A conversion technique. This test series, like the PSK test series, was conducted in the laboratory at the Digital Communications Experimental Facility (DICEF), Rome Air Devepoment Center (RADC), Griffiss Air Force Base, Rome, New York. These tests were conducted on January 12th and 13th, 1976.

The test configuration used to determine the effects of CVSD A/D/A processing on the MD-701's performance was identical to that used in the PSK modem tests. The output of the MD-701 transmitter was set at -10 dBm while the received signal was set at -16 dBm by the unit amplifier following the CVSD conversion process. These signal levels correspond to the nominal signal levels as used in the overseas AUTODIN application.

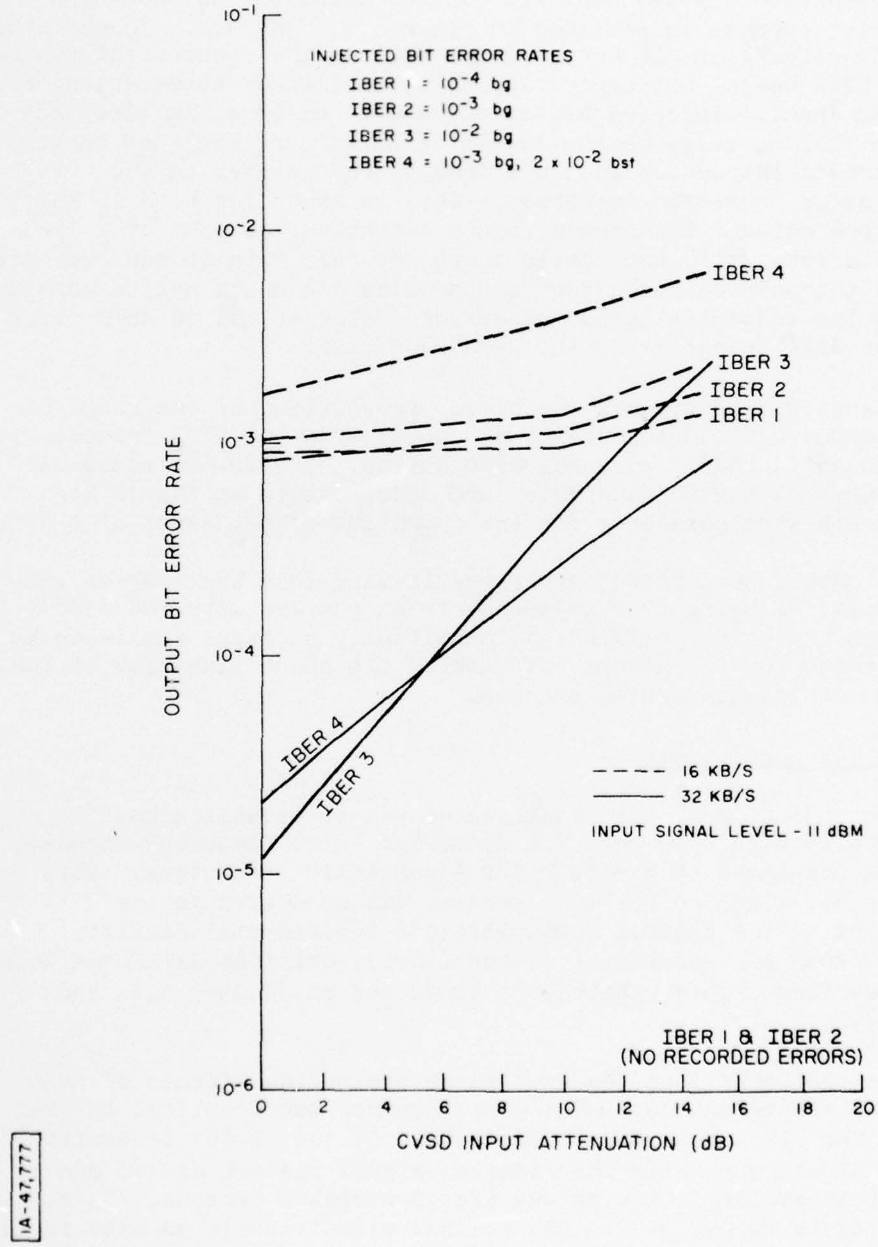


Figure 3.1 CVSD/USC-10 TEST RESULTS AT 1200 BAUD RATE

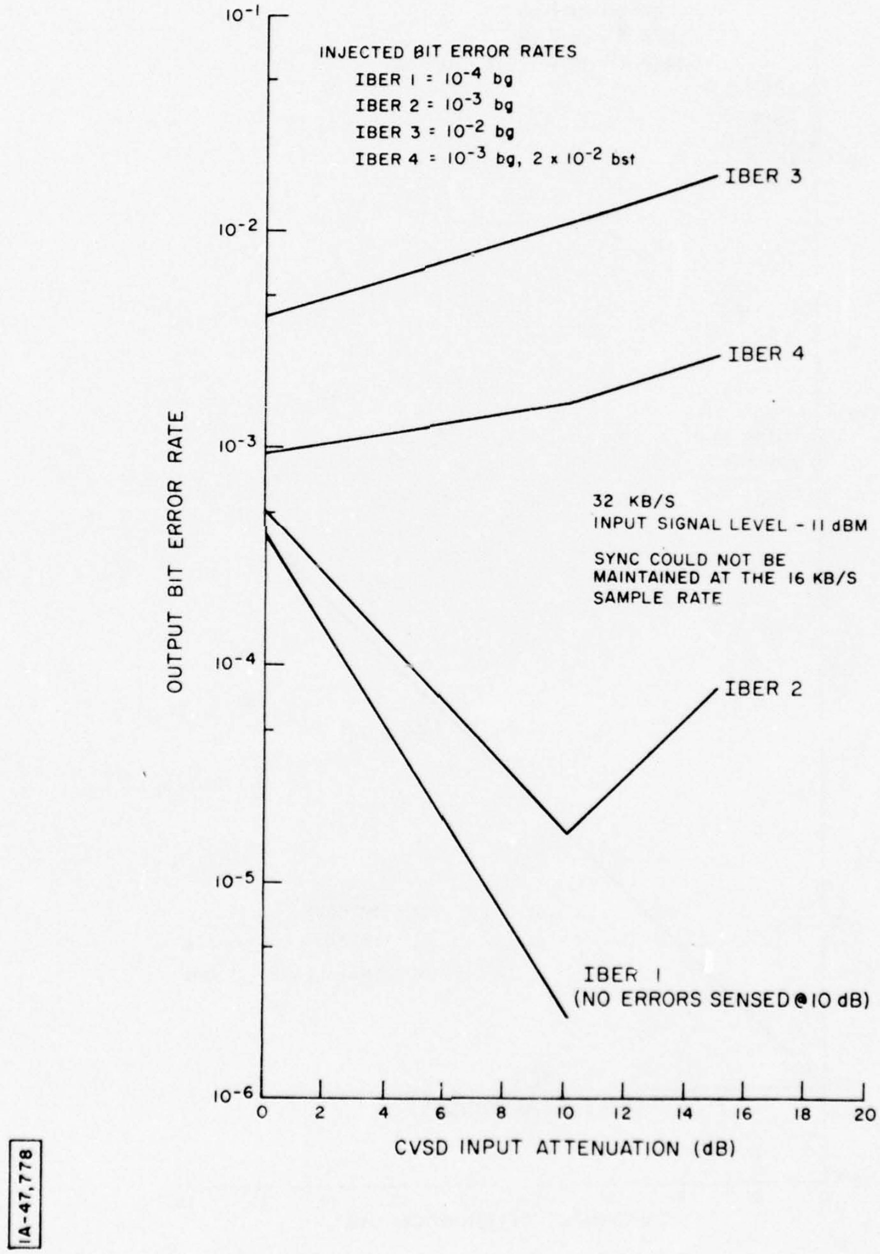


Figure 3.2 CVSD/USC-10 TEST RESULTS AT 2400 BAUD RATE

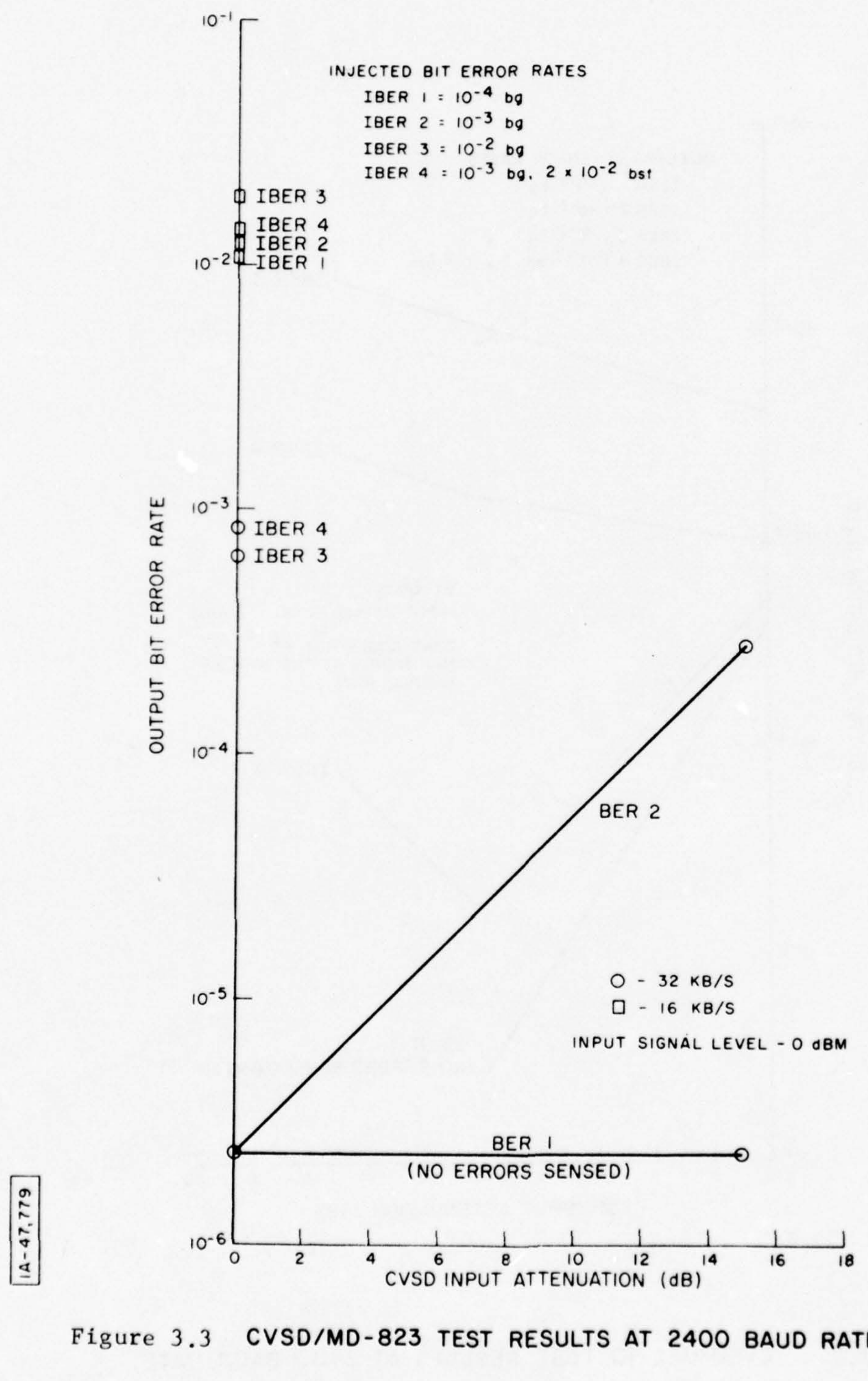


Figure 3.3 **CVSD/MD-823 TEST RESULTS AT 2400 BAUD RATE**

The range of performance for the MD-701 modem when a CVSD device is used to provide the A/D/A conversion function is shown in Figures 3.4 and 3.5. The former figure shows the resulting system bit error rate as a function of an inserted digital error rate between the CVSD encoder and decoder for operation at a 1200 baud data rate. Figure 3.5 shows the same data for the same range of variables when a 2400 baud data rate was used.

3.5 MD-701 Modem Laboratory Tests

As discussed in the previous section, the performance of this modem for various rates of CVSD digital channel bit errors was investigated at RADC, Rome, New York. At the conclusion of these tests the modem used was returned to MITRE for more extensive laboratory tests. The objective of these additional tests was to gain further insight into the Modem/CVSD interface problem, particularly with regard to the effects of additive Gaussian noise and tandem CVSD conversions.

The basic test configuration used in the laboratory is shown in Figure 3.6. The mixer box allowed for the controlled addition of band-limited Gaussian noise to the modem's audio output, and consequently adjusted the S/N ratio at the input to the CVSD coder. As in the previous tests, provision was made to vary the operating point (input level) of the coder, with 0 dB attenuation representing a -10 dBm input level in the absence of noise. Digital bit errors were injected into the CVSD digital channel as discussed earlier. A distortion analyzer was connected to the input and output of the CVSD coder/decoder chain to investigate the decrease in S/N ratio caused by the CVSD process and the digital error generator. Also, the modem receiver's FM discriminator output and recovered clock were applied to a camera-equipped oscilloscope in order to record the "eye-pattern" of the received signal. The oscillographs of these eye-patterns could then be correlated with the various corrupting factors in the system to determine the character of their effect on data transmission. As shown in the dashed portion of the figure, the case of multiple CVSD conversions was also investigated. However, to minimize the number of variables in the test, the input to the tandem CVSD coder was held at -10 dBm in the absence of noise. In both the single and double conversion cases the input level to the receive side of the modem was compensated to a level of -16 dBm.

Representative results of the tests performed on the two CVSD devices for the case of a single CVSD A/D/A conversion are shown in Figures 3.7 through 3.14. Figure 3.7 depicts the system bit error rate for 1200 baud modem operation as a function of CVSD operating

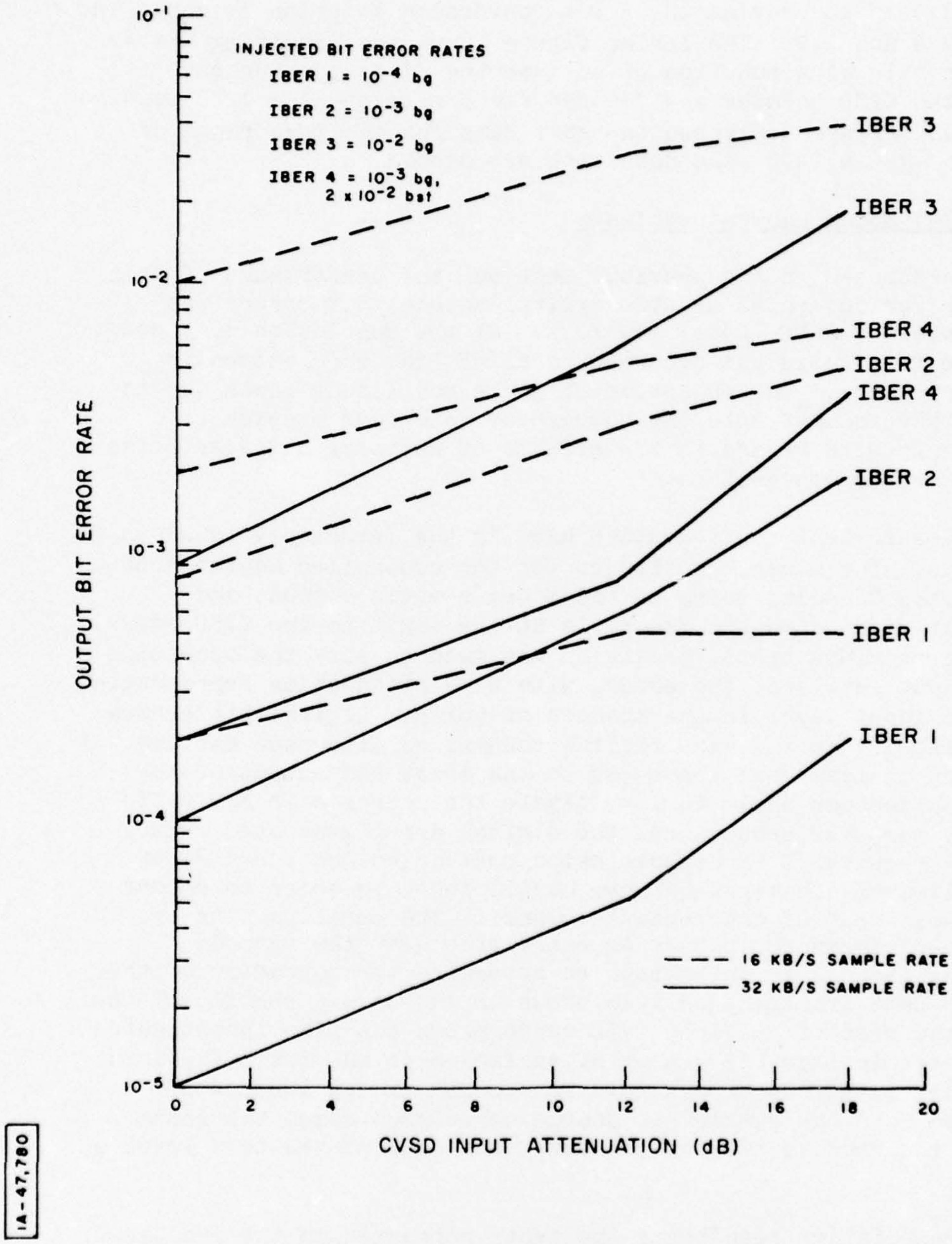


Figure 3.4 CVSD/MD-701 TEST RESULTS AT 1200 BAUD RATE
OUTPUT BIT ERROR RATE vs. INPUT ATTENUATION
FOR VARIOUS INJECTED BIT ERROR RATES

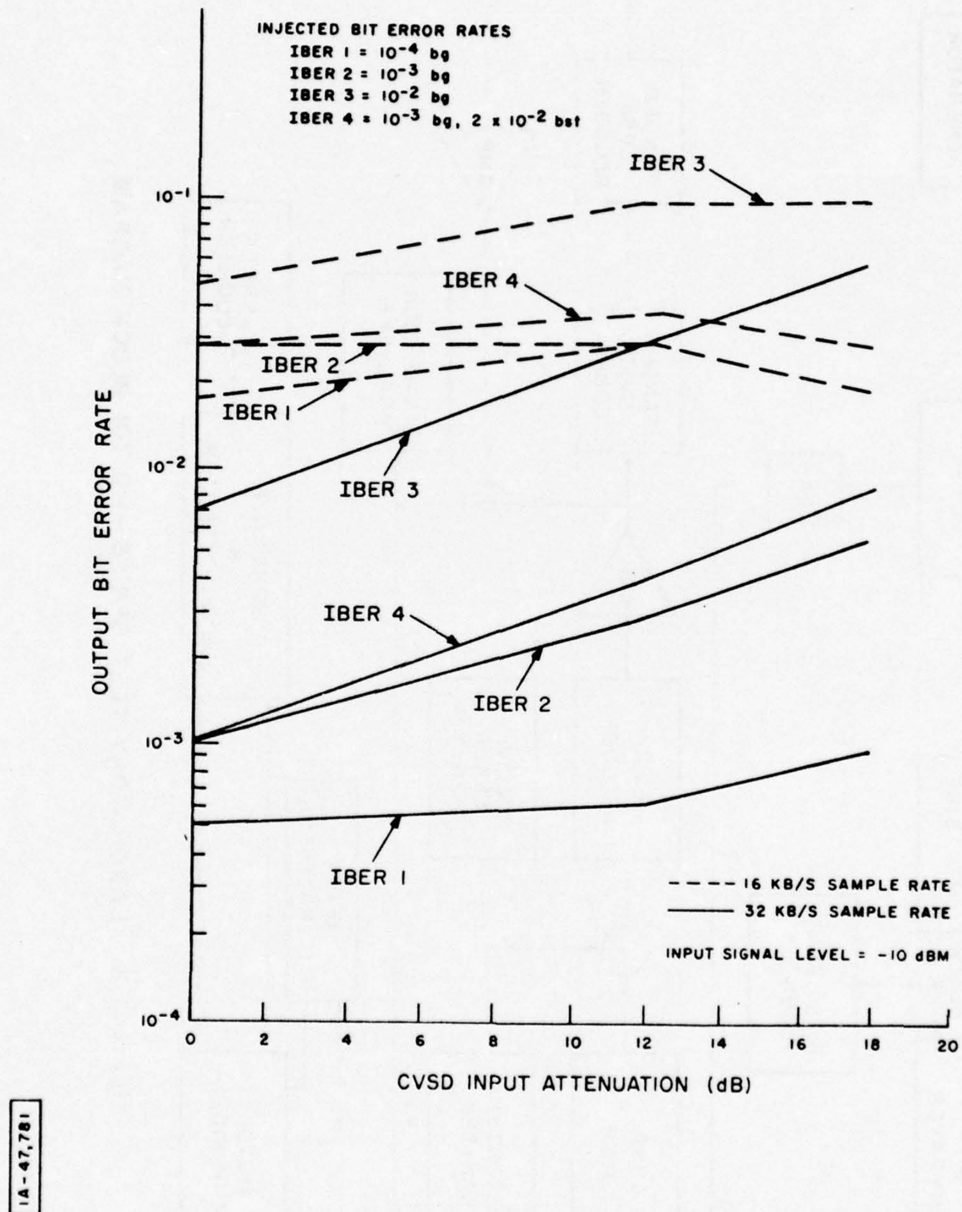


Figure 3.5 CVSD/MD-701 TEST RESULTS AT 2400 BAUD RATE OUTPUT BIT ERROR RATE vs. INPUT ATTENUATION FOR VARIOUS INJECTED BIT ERROR RATES

IA-47,782

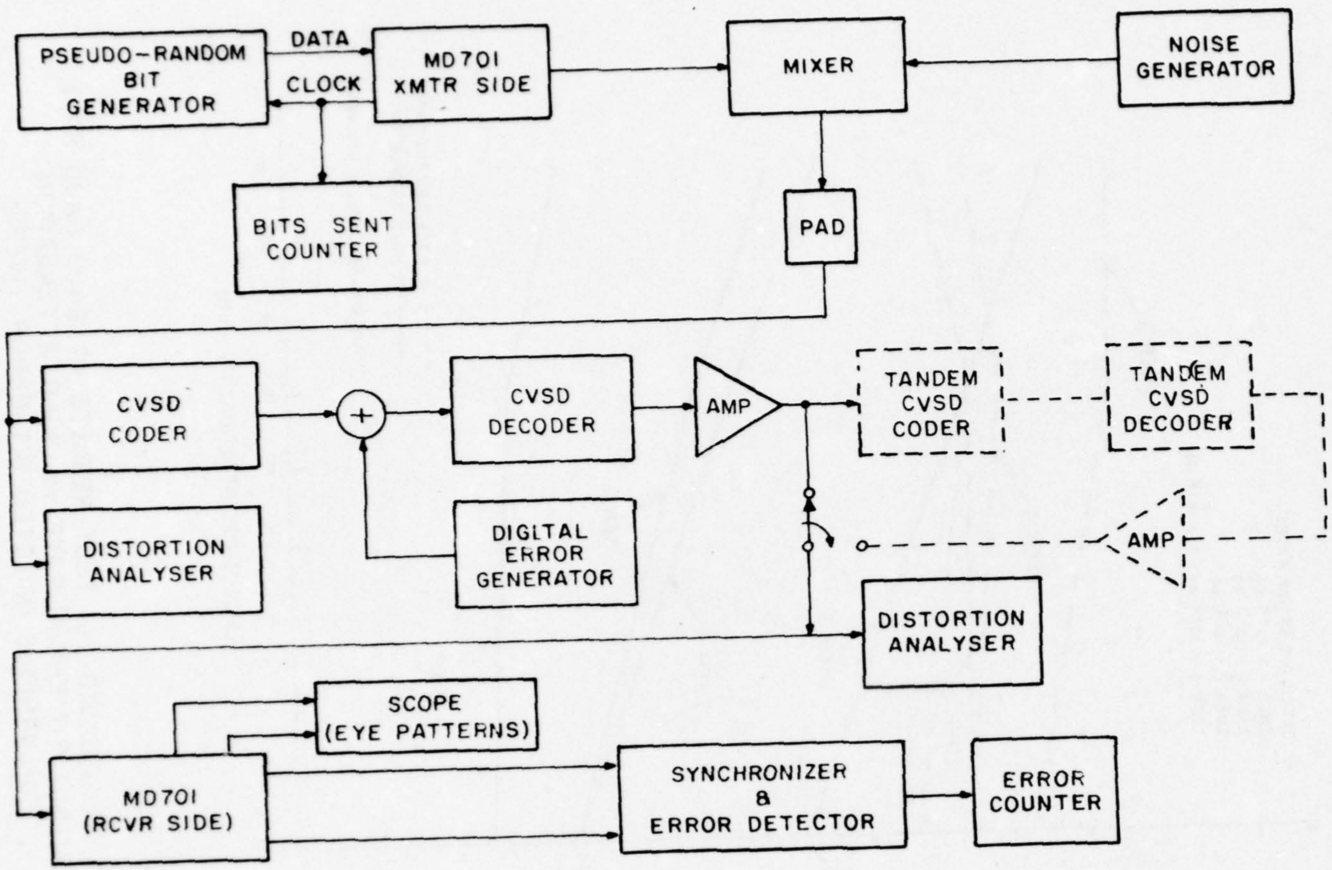


Figure 3.6 LABORATORY TEST SERIES - MD 701 BLOCK DIAGRAM

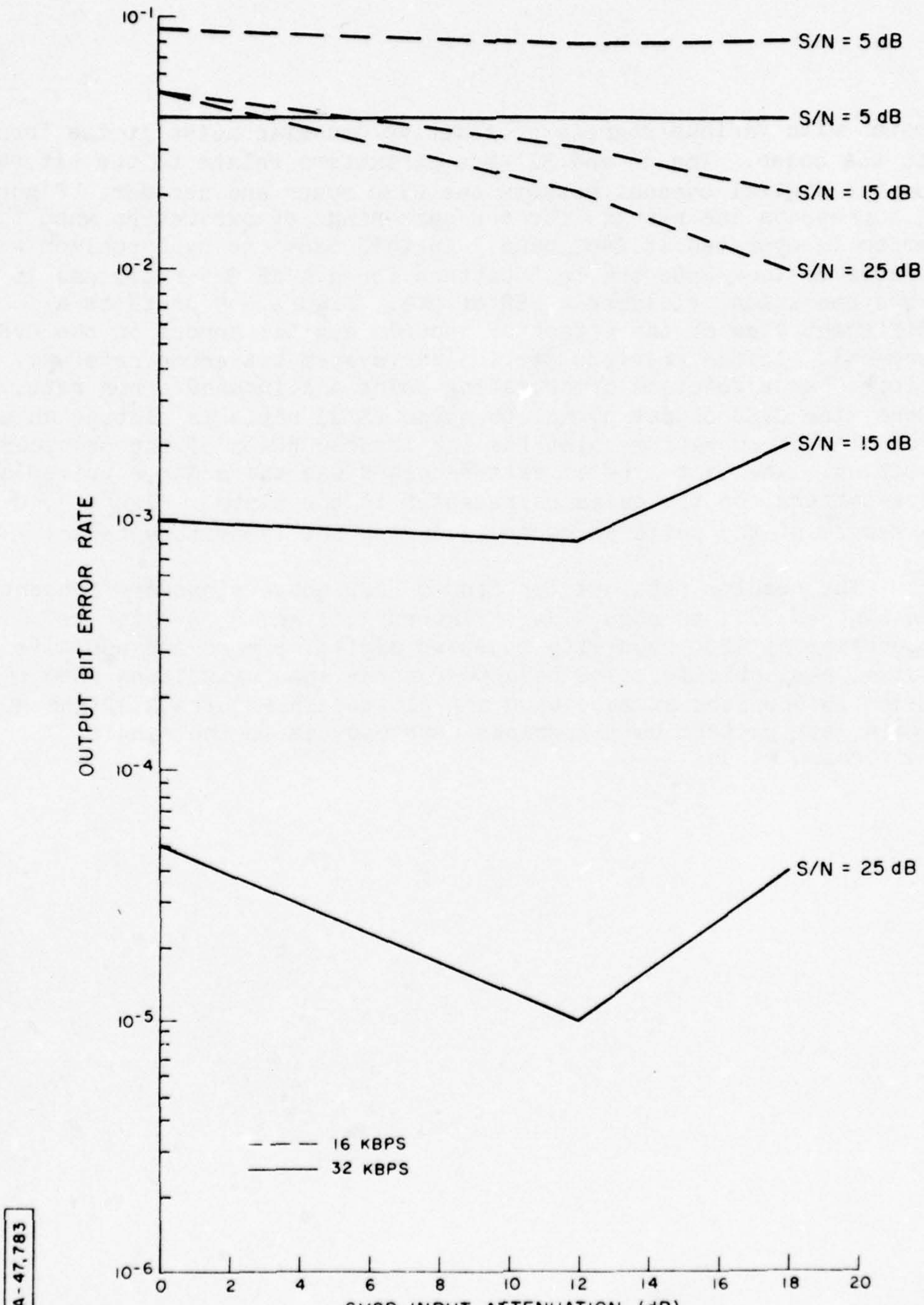


Figure 3.7 CVSD/MD-701 TEST RESULTS AT 1200 BAUD RATE OUTPUT BIT ERROR RATES vs. INPUT ATTENUATION FOR VARIOUS S/N RATIOS

point with various degrees of additive Gaussian noise at the input to the coder. The 16 and 32 kb/s parameters relate to the bit rate on the digital channel between the CVSD coder and decoder. Figure 3.8 presents the results for the same range of parameters when the modem is operated at 2400 baud. In this case the synchronizer was unable to lock onto the test pattern for a 5 dB S/N ratio and 16 kb/s operation, yielding a BER of 0.5. Figure 3.9 presents a different view of the effect of induced digital errors on the CVSD process. In the previous section the system bit error rate was plotted as a function of operating point and induced error rate. Here the CVSD output signal to noise (S/N) ratio is plotted as a function of operating point for the induced BER's of the previous section. The last type of data recorded was the modem receiver's eye-pattern for the cases represented in the plots. Figure 3.10 is a sample of the patterns recorded during the laboratory tests.

The results obtained for tandem CVSD conversions are presented in Figures 3.11 through 3.14. Figures 3.11 and 3.13 refer to operation at 1200 baud with injected digital errors and additive noise, respectively. The results for the same situations when the modem is operated at 2400 baud are plotted in Figures 3.12 and 3.14. Again, eye-pattern oscillographs were made as in the single conversion cases.

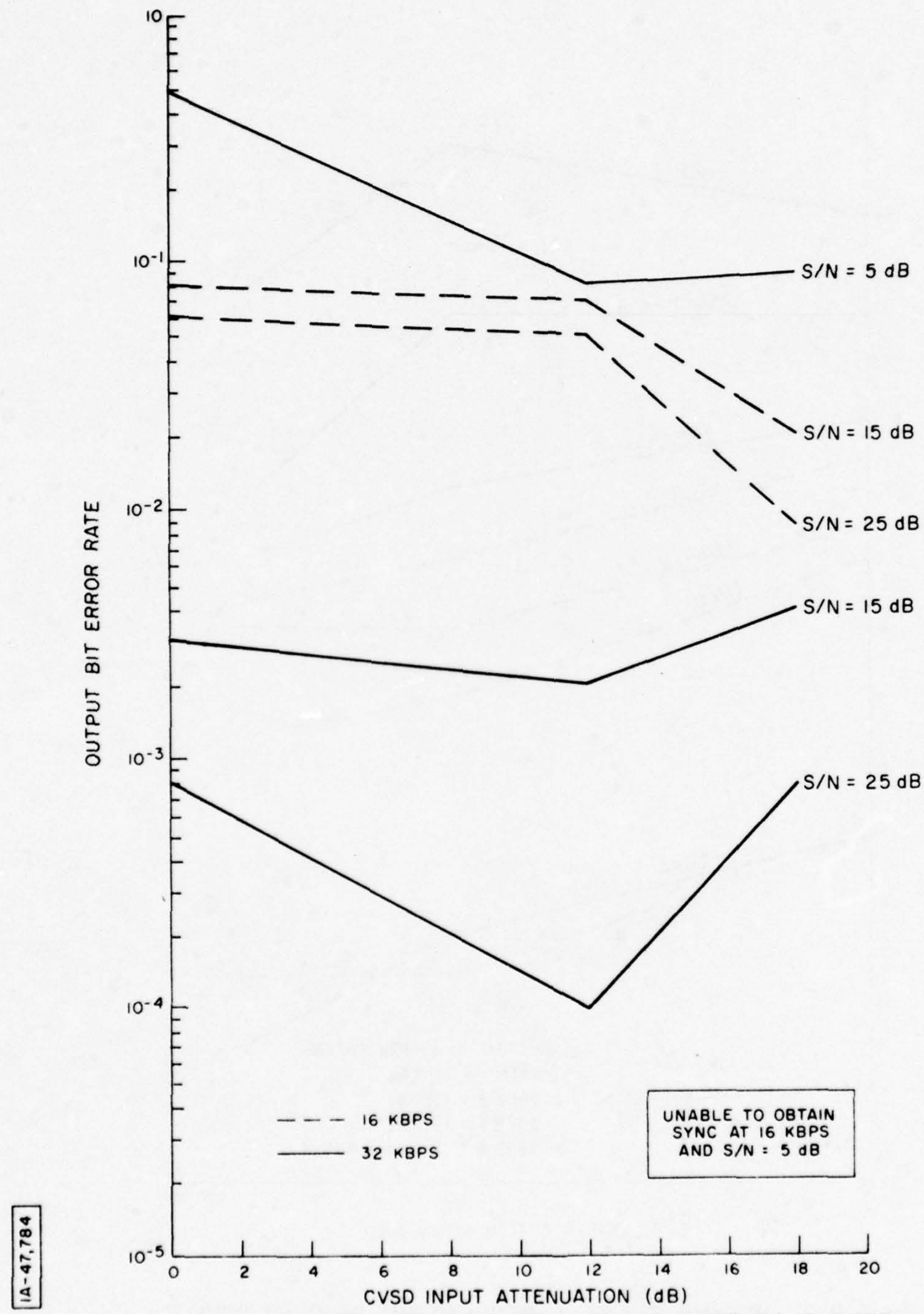


Figure 3.8 CVSD/MD-701 TEST RESULTS AT 2400 BAUD RATE OUTPUT BIT ERROR RATE vs. INPUT ATTENUATION FOR VARIOUS S/N RATIOS

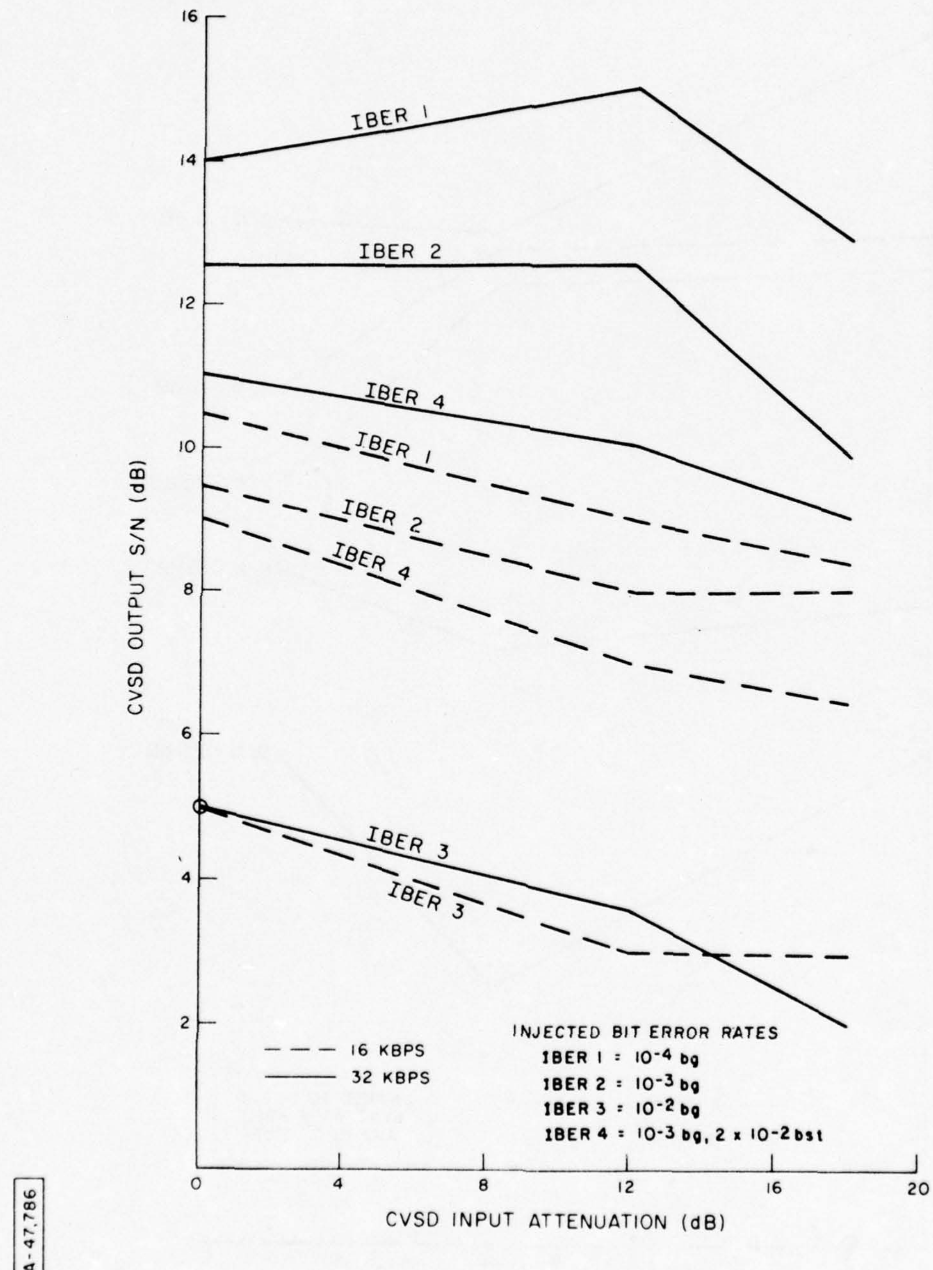
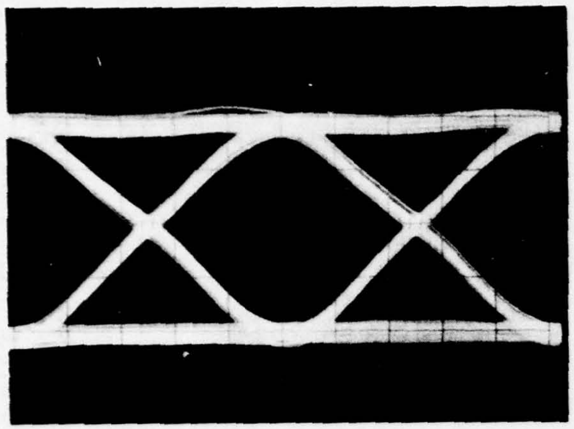
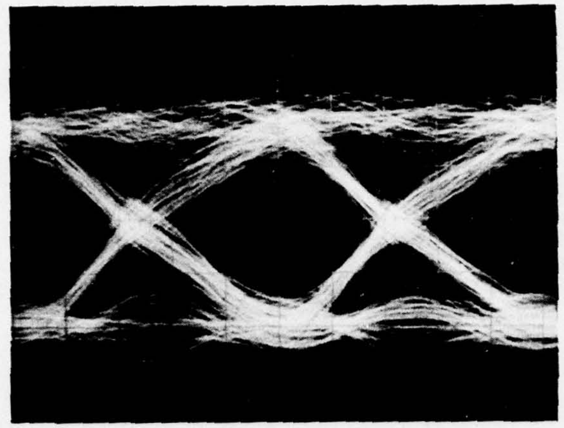


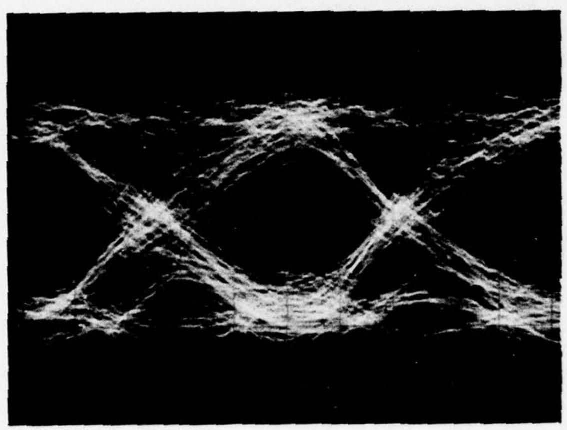
Figure 3.9 CVSD/MD-701 TEST RESULTS FOR 2400 HZ TONE OUTPUT S/N RATIO vs. INPUT ATTENUATION FOR VARIOUS INJECTED BIT ERROR RATES



32 KBS
1200 BAUD
NO DIGITAL NOISE
NO ANALOG NOISE
NO CVSD



32 KBS
1200 BAUD
NO DIGITAL NOISE
NO ANALOG NOISE
NSA CVSD IN LOOP



32 KBS
1200 BAUD
NO ANALOG NOISE
INJECTED DIGITAL ERROR RATE = 10^{-2} bg
NSA CVSD IN LOOP

Figure 3.10 Oscilloscope Eye Patterns

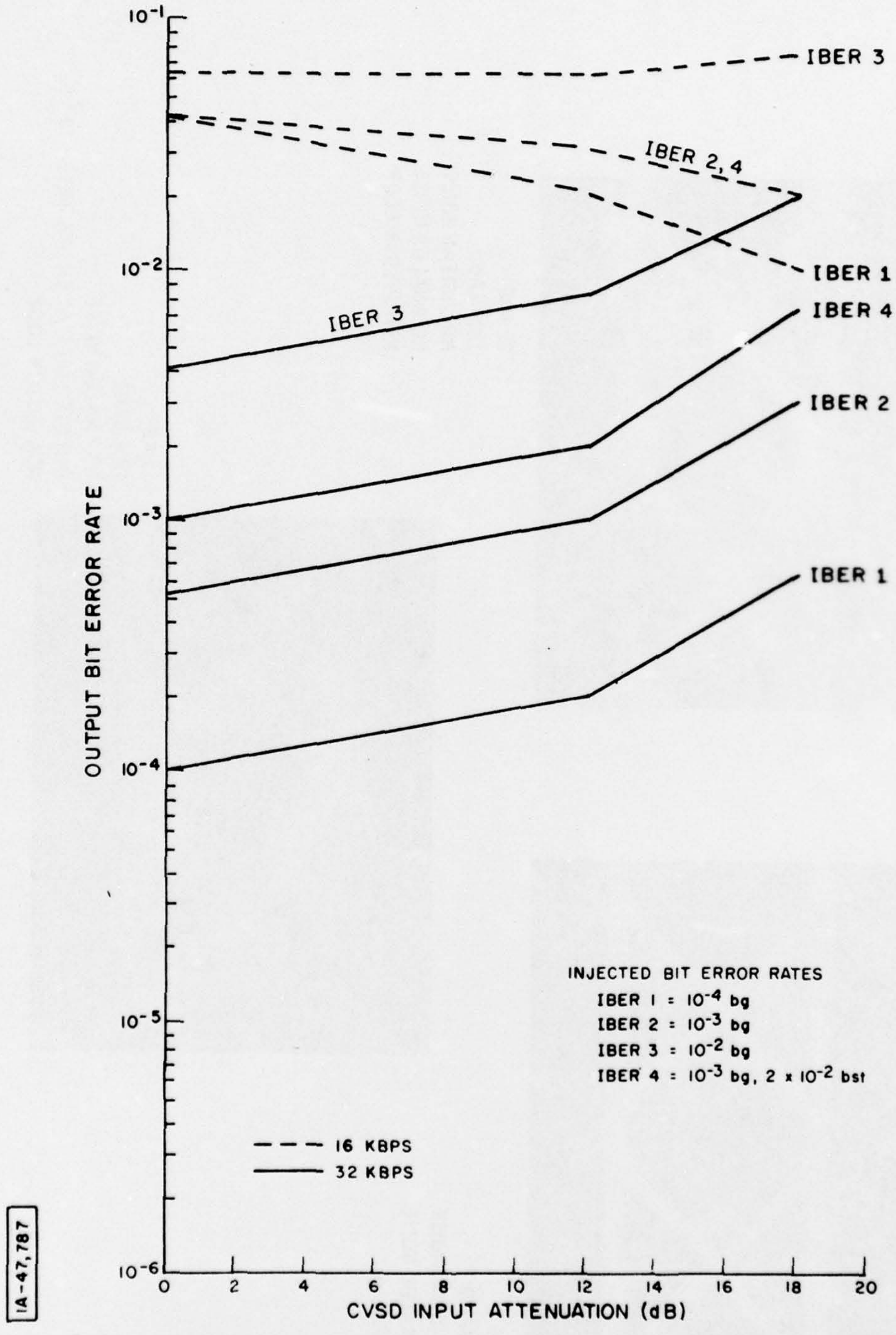


Figure 3.11 TANDEM CVSD/MD-701 TEST RESULTS AT 1200 BAUD RATE OUTPUT BIT ERROR RATES vs. INPUT ATTENUATION FOR VARIOUS INJECTED BIT ERROR RATES

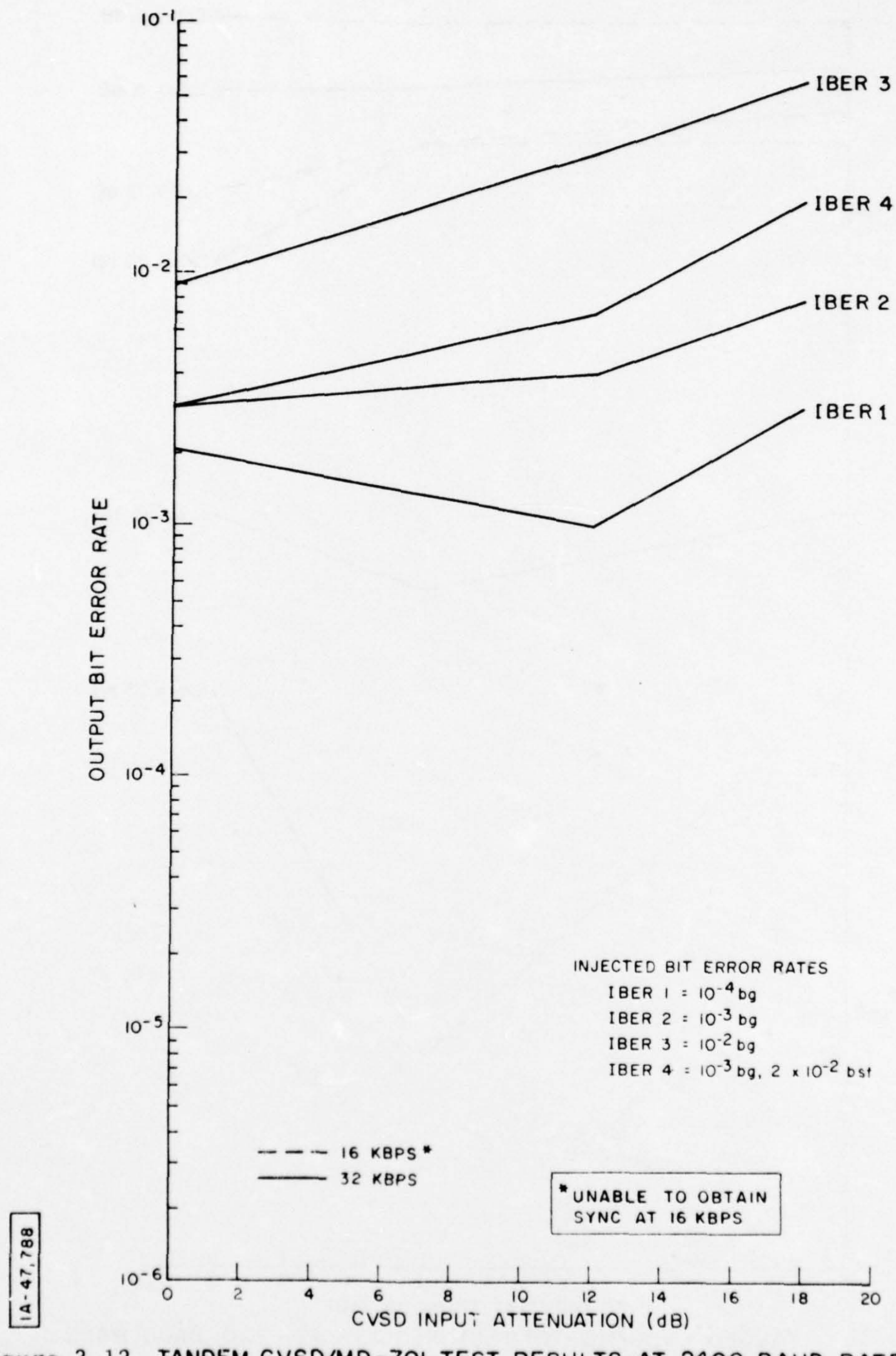


Figure 3.12 TANDEM CVSD/MD-701 TEST RESULTS AT 2400 BAUD RATE OUTPUT BIT ERROR RATES vs. INPUT ATTENUATION FOR VARIOUS INJECTED BIT ERROR RATES

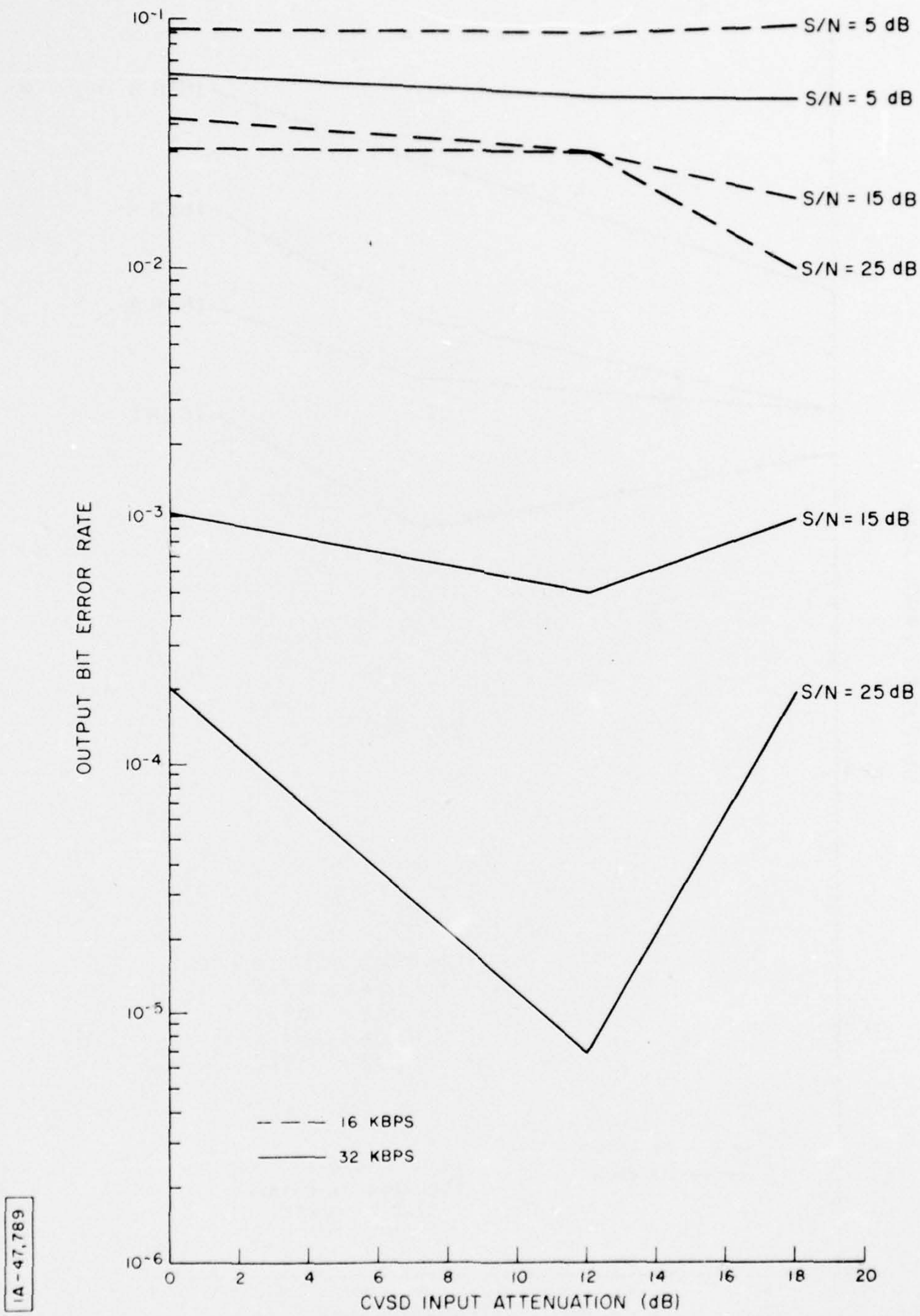


Figure 3.13 TANDEM CVSD/MD-701 TEST RESULTS AT 1200 BAUD RATE OUTPUT BIT ERROR RATE vs INPUT ATTENUATION FOR VARIOUS S/N RATIOS

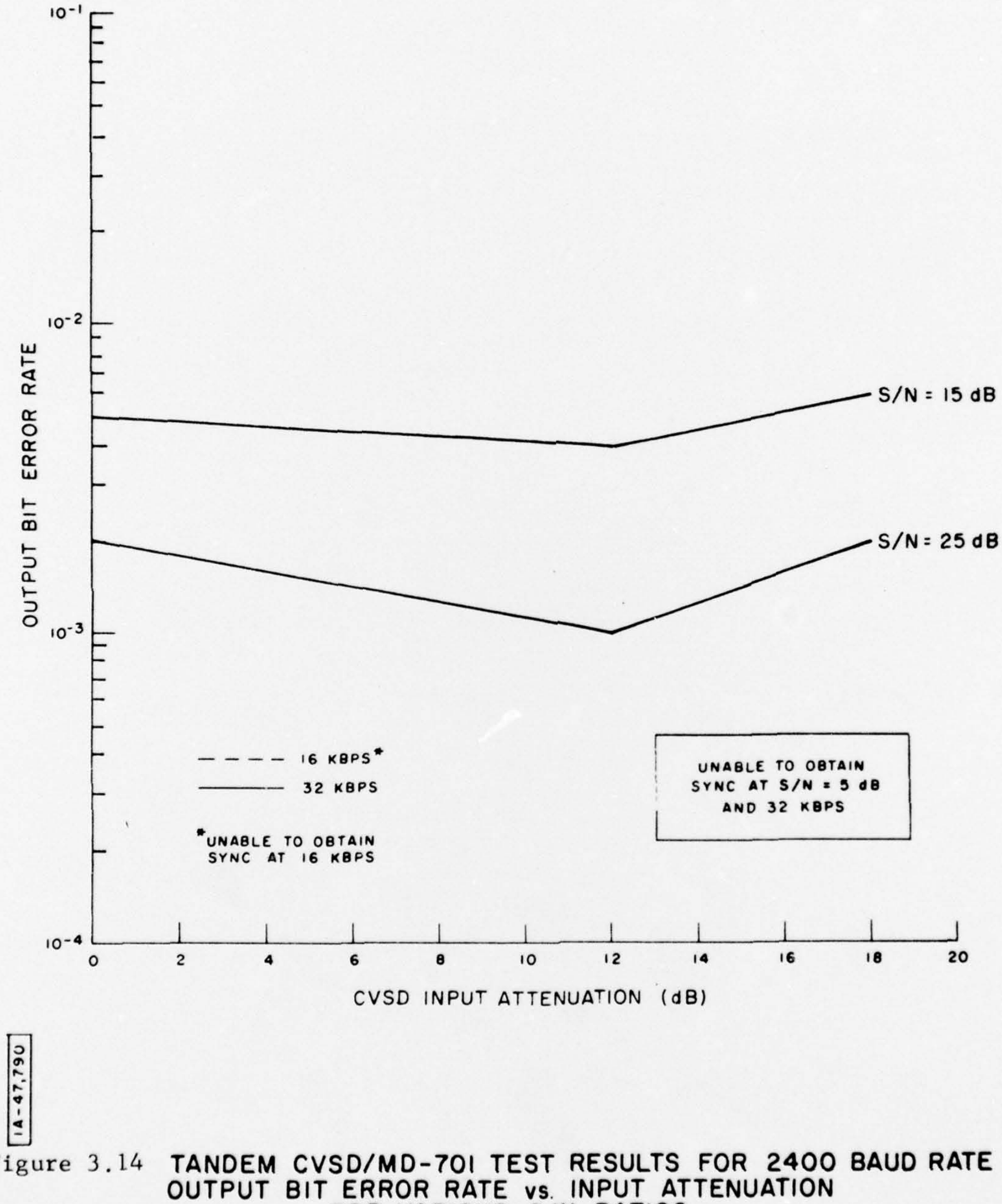


Figure 3.14 TANDEM CVSD/MD-701 TEST RESULTS FOR 2400 BAUD RATE OUTPUT BIT ERROR RATE vs. INPUT ATTENUATION FOR VARIOUS S/N RATIOS

4.0 ANALOG DEVICES TEST SERIES

4.1 DTMF Signaling and Supervision in the TTC-30 Interface

The overall objective of this test series was to determine the capability of a CVSD type device to process supervisory and Dual Tone Multiple Frequency (DTMF) signals from a military telephone set (TA-341) in an operational 407-L system, and to analyze the effects of this CVSD processing on the ability of the TTC-30 switch to recognize and act on these signals. Specifically, the effects of clock rate, amplitude level at the CVSD input, and injected errors were to be studied. In addition, tone duration at the output of the DTMF signal source was established as a parameter of these tests.

The TA-341 telephone set was utilized as the inventory item signal source for this test. This telephone is a transistorized semi-ruggedized desk instrument developed for the Seventh Army Tactical Switching System. The AC signalling scheme provides compatibility with the AN/TTC-25, the AN/TTC-30, and any similarly equipped electronic central office. This telephone set is used to originate and receive calls via the associated switching facility, or may be used in a back-to-back configuration with another TA-341 telephone set for point-to-point service. It is a four-wire instrument, and uses local battery (internal) power. Voice-frequency tones are used for digital and supervisory signaling to and from the switch facility. A list of the TA-341 telephone characteristics is shown in Table 4.1.

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Table 4.1

TA-341 Telephone Set Characteristics

Seize Tone level (2250 Hz)	-4 dBm .± 2 dB
Release tone level (2600 Hz)	-4 dBm ±2 dB
Dual tone signalling levels (DTMF)	-4 dBm ±2 dB
Point-to-point ring signal tone	570 Hz ±2%
Seize tone	2250 Hz ±1.5%
Release tone	2600 Hz ±1.5%
Recall/line priority tone	941 + 1209 Hz ±1.5%
Conference control tone	941 + 1477 Hz ±1.5%
Digit tones:	
1	697 + 1209 Hz ±1.5%
2	697 + 1336 Hz ±1.5%
3	697 + 1477 Hz ±1.5%
4	770 + 1209 Hz ±1.5%
5	770 + 1336 Hz ±1.5%
6	770 + 1477 Hz ±1.5%
7	852 + 1209 Hz ±1.5%
8	852 + 1336 Hz ±1.5%
9	852 + 1447 Hz ±1.5%
0	941 + 1336 Hz ±1.5%

A Mode Selector Switch on the unit provides three modes of operation: AC supervision, point-to-point, and DC supervision. AC supervision was used for all of the tests reported in this paper.

A photograph of the test equipment which was assembled for these tests is shown in Figure 4.1. All of the test equipment (including the CVSD unit under test) was installed on a portable tray, or pallet, which could be easily transported to the CRC test site. The equipment was arranged on the pallet with all interconnecting cables in place and with the controls easily accessible so that it was not necessary to remove any of the equipment from the pallet during the tests. A diagram of the test setup was shown earlier in Figure 2.2.

A TA-341 telephone set was modified to permit it to be coupled to a pulse duration controller which controlled the duration of the DTMF and supervisory signals generated within the telephone set. A set of switches on the controller permitted the selection of various signal durations from 40 milliseconds to 1.44 seconds. A bypass switch on the controller allowed the telephone to bypass the control unit and return to normal operation.

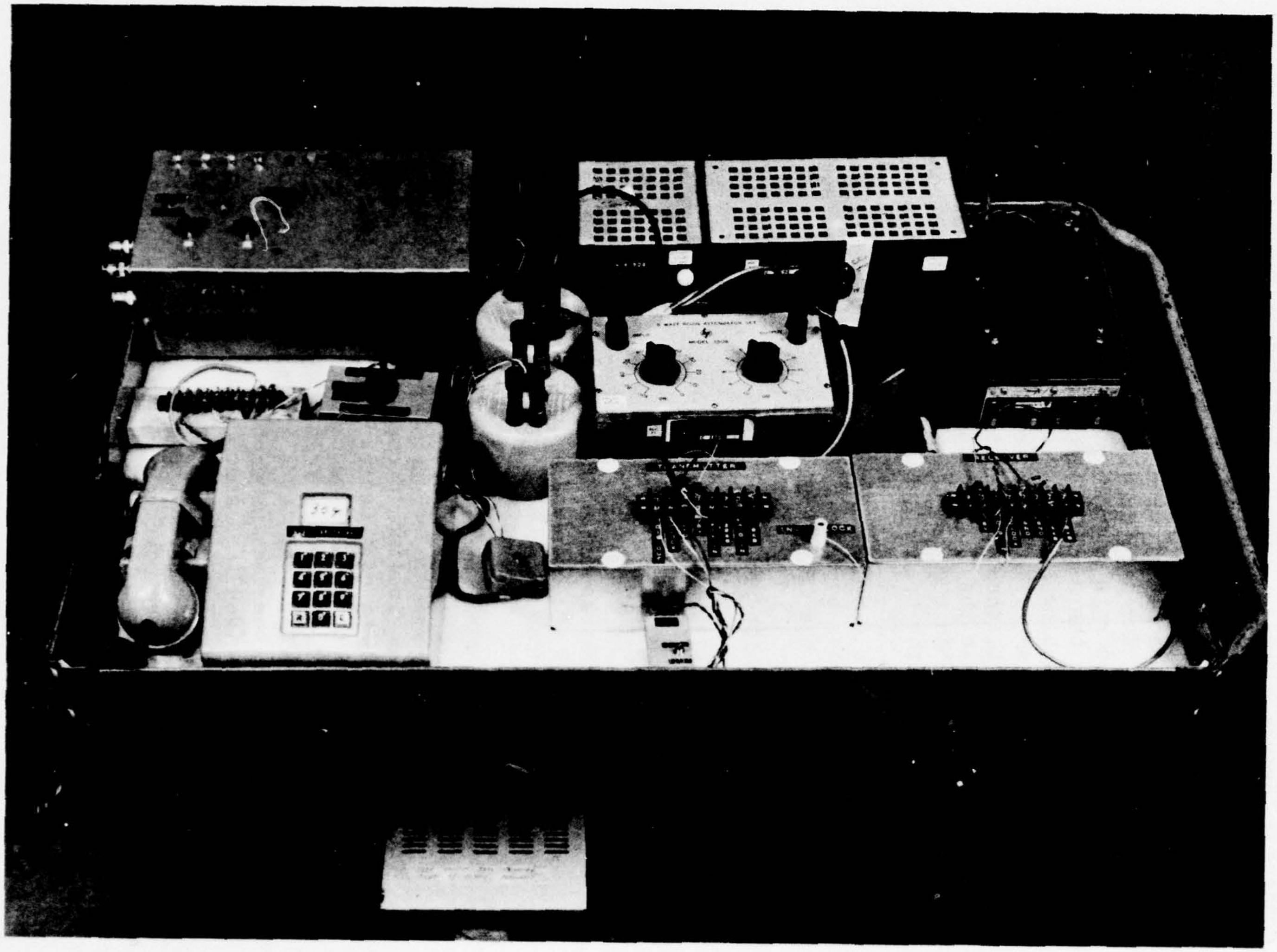

Figure 4.1 ADM/D Test Items and Support Equipment

The telephone transmit leads as shown earlier in Figure 2.2 were connected through a bypass switch in the CVSD test equipment to the primary winding of a 600 ohm transformer, the secondary winding of which was connected to a variable Hewlett-Packard 350 B attenuator. After passing through the attenuator, the DTMF and supervisory signals from the telephone set were fed to the CVSD encoder where they were digitized. The digital signals were then passed through a burst/background error rate generator which injected errors at selectable rates into the digital signal stream. The signal was then reconverted to analog by the CVSD decoder and amplified by a General Radio 1206-B amplifier back to the level at which it emerged from the telephone set, thus compensating for signal level attenuation incurred in the test setup. The signal was finally coupled through a second 600 ohm transformer and the second half of the bypass switch to the transmit leads to the TTC-30 switch. The receive pair from the TTC-30 was fed directly to the TA-341 telephone set. With the bypass switch in the bypass position, the telephone transmit leads bypassed the entire CVSD test equipment and connected directly to the CRC communication system.

The parameters which were studied in this test series included:

1. Clock rate: 32 kHz and 16 kHz

2. Signal duration: 140 ms and 60 ms

3. Input signal attenuation: 0 dB, 12 dB and 18 dB

4. Background error rate; 1×10^{-4}, 1×10^{-3}, 1×10^{-2}

5. Burst/background error rate: 2×10^{-2} burst plus 1×10^{-3} background

The test pallet was located in the TSQ-91 operations center at one of the operator positions. One person operated the test equipment, varying the parameters according to the test tree, and dialing the telephone test numbers from the TA-341 telephone set on the pallet. Each number was dialed a minimum of five times for every change in one of the test parameters. The numbers used covered all ten digits (0-9). A second member of the test team was located remotely in the TTC-30 van, and he monitored and recorded the numbers as they were being interpreted by the TTC-30 switch. These received numbers were compared with the dialed numbers to determine the processing inaccuracies introduced by the CVSD conversion conditions. The supervisory signals were also tested in a similar manner.

The results of the DTMF signal testing are shown in Figure 4.2, and are summarized below:

> With no burst/background errors induced, the DTMF dialing produced no errors at either 32 kHz or 16 kHz clock rates for any of the signal input attenuations used.
>
> With 1.0% induced background errors there were no errors produced by the dialing at the 32 kb/s clock rate over the complete range of input attenuation values.
>
> With 1.0% induced background errors and 0 dB attenuation of input signal there were no errors produced by the dialing at the 16 kb/s clock rate. For other values of attenuation and higher induced error rates, dialing errors were appreciable, as shown in Figure 4.2.
>
> With 3.0% induced background errors and 18 dB input signal attenuation, the dialing errors increased to 100% at both 32 kHz and 16 kHz.

The results of the supervisory signal processing tests are shown in Table 4.2.

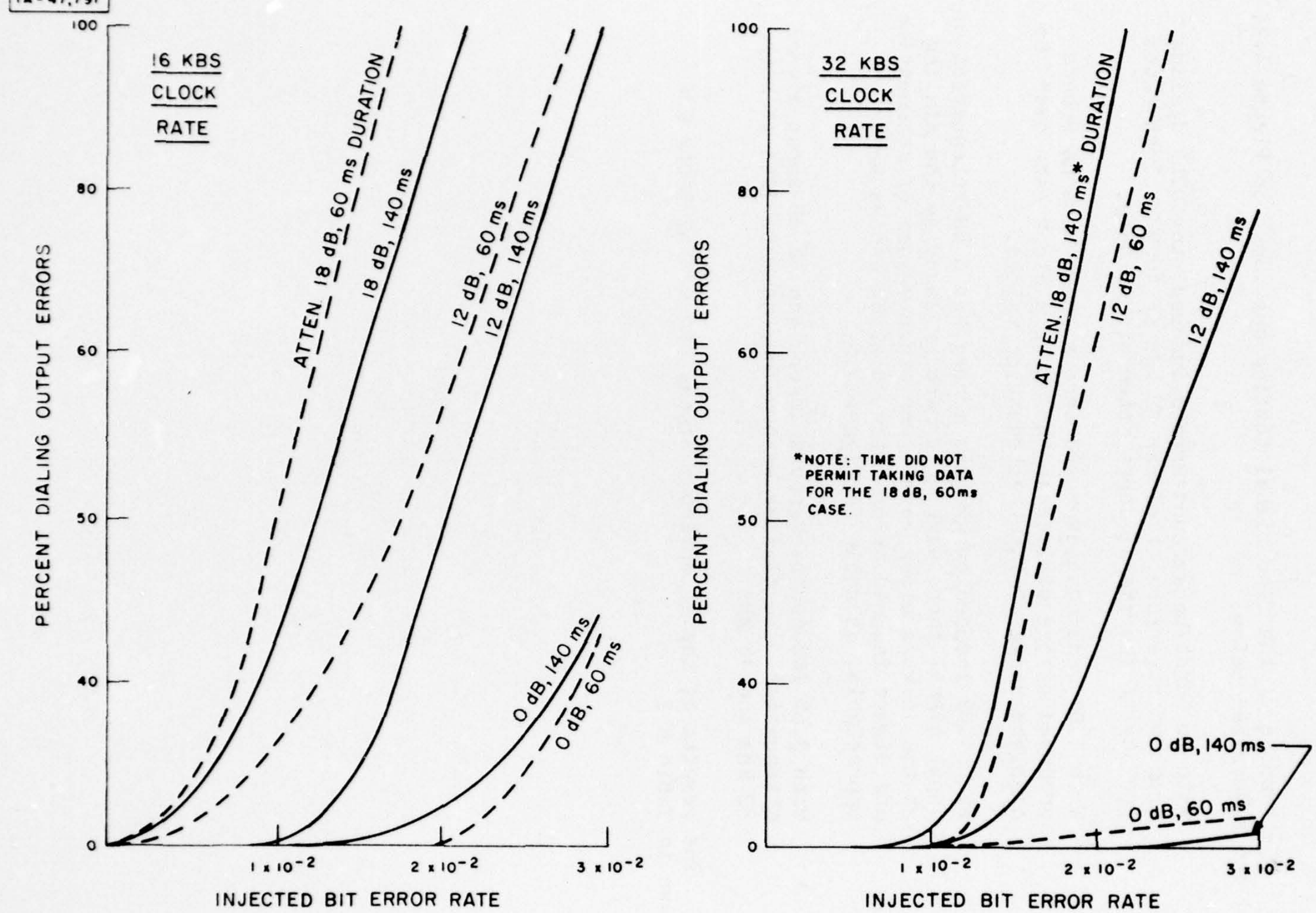

Figure 4.2 **RESULTS OF DTMF TESTS**

Table 4.2 Results of Supervisory Signal Tests

	32 kHz Clock Rate		16 kHz Clock Rate	
	Input Signal Attenuation	No Bkgd. Noise	Input Signal Attenuation	No Bkgd. Noise
ON HOOK 2600 Hz	0 dB	Go	0 dB	Go
	10 dB	Go	10 dB	Go
	15 dB	Go	15 dB	No Go
OFF HOOK 2250 Hz	0 dB	Go	0 dB	No Go
	10 dB	Go	10 dB	Go
	15 dB	Go	15 dB	Go

Note: High injected error rates ($\geq 1\%$ Background) inhibited supervisory signaling

5.0 SUMMARY OBSERVATIONS AND IMPLICATIONS FOR TRI-TAC APPLICATION

Considering the results of the test series and a review of available literature offering augmenting data, the following observations may be made.

5.1 Operating Point Sensitivity

The results of the tests indicate that the CVSD performance is sensitive to input signal level. For modem interfaces, a shift from the normal operating point may be necessary for optimum CVSD performance. This action could be coupled with the introduction of an automatic operating point adjustment on the CVSD input for dynamic range compensation.

5.2 Speech Parameters vs. Quasi-Analog Signal Parameters

The algorithms which formed the basis for the design of the test items supplied did not impose specifications on the phase linearity of the output filters. This area offers an avenue for potential improvement in processing PSK modem signals.

5.3 Acceptable Signal Range Shrinkage for Multiple Conversions

Considering the ESD/MITRE test series and those of bibliography item 2, it is apparent that the range of signal levels over which acceptable performance is achievable reduces with multiple conversions.

5.4 Performance Parameter Considerations

a. 16 kb/s Clock Rate - Performance of CVSD at 16 kb/s sample rate was unacceptable for most interfaces tested and suffered severe dynamic range restrictions for those interfaces wherein some degree of successful operation was achieved. Therefore its application as a general purpose converter at this clock rate is severely limited.

b. 32 kb/s Clock Rate - For a single conversion (A-D/D-A), acceptable operation was achieved for all interfaces tested for baud rates up to 1200/second. Inherent in this statement are the assumptions that operating point flexibility and control are available at the system interface, and that the injected error statistics applied, output error rate realized and resulting dynamic range are acceptable to the user in his application. Reference should be made to performance data for specific cases.

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Having made the foregoing observations, it is apparent that there are some open questions to be considered:

1. What degree of improvement in CVSD quasi-analog signal performance can be achieved by placing constraints on the phase linearity of input and output filters?

2. What shall be the form of an operating point control for CVSD interface with quasi-analog signal sources?

3. What are the TRI-TAC architectural constraints on multiple CVSD conversions? Is the resulting dynamic range acceptable?

In concluding this paper, it is noted that the CVSD process may offer a viable interim approach for a simple and inexpensive quasi-analog signal conversion technique, given that the observations stated earlier are carefully considered in its application during the phased introduction of TRI-TAC digital systems.

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5. TRI-TAC Specification TT-B1-2101-0039, "Performance Specification for a Family of Universal Synchronous Multiplexers," 16 January 1976.